

102

The diagram illustrates a digital PLL system. It consists of two parallel processing paths for the I and Q inputs. Each path starts with a 'Sqrt Nyquist Filter', followed by a 'x/sinx' block, then a 'D/A' block, and finally an 'LPF' block. The outputs of the LPFs are multiplied by  $\cos 2\pi f_c t$  and  $\sin 2\pi f_c t$  respectively. The results are then combined to produce the final output.

Figure 1A A simplified PSK transmitter.

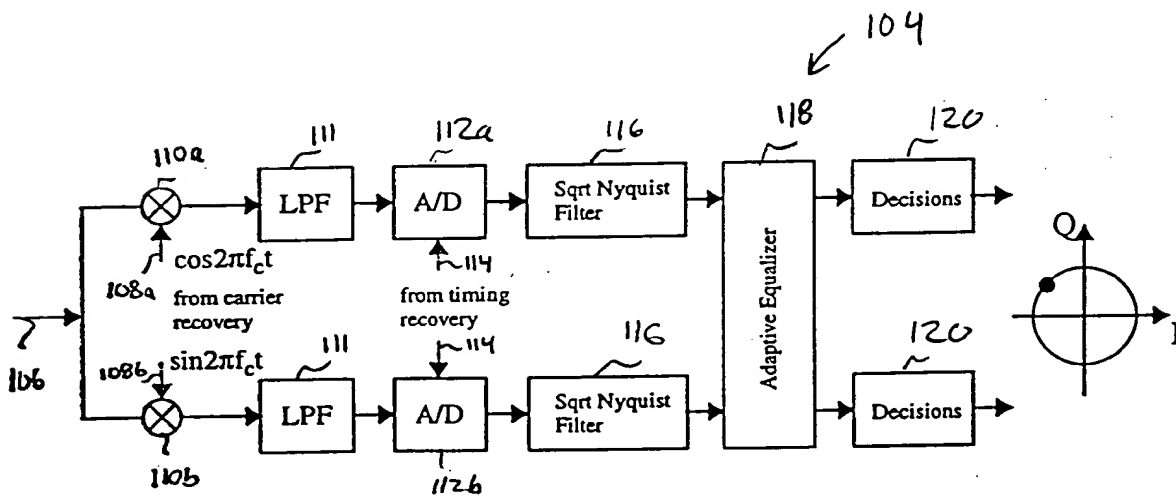


Figure 10 A simplified PSK receiver.

126

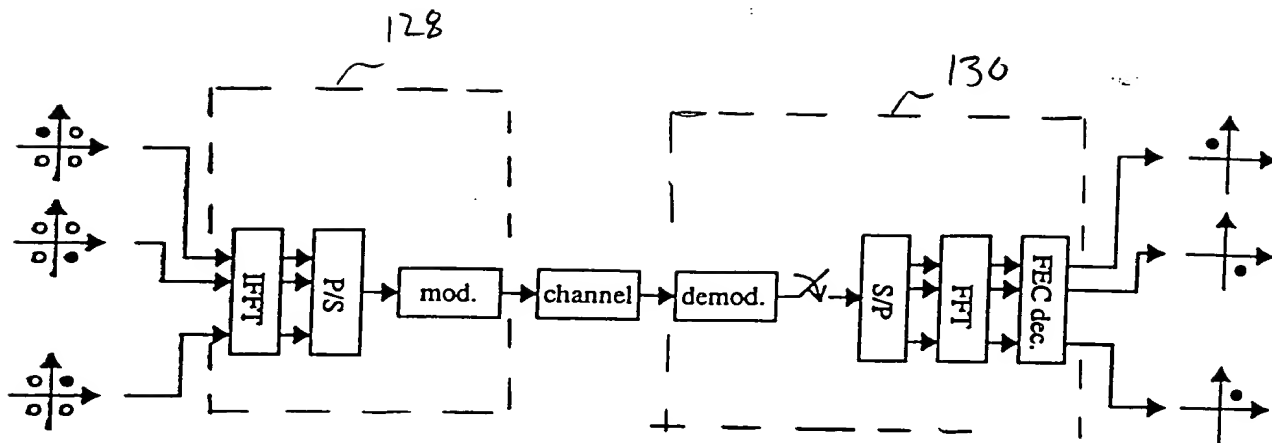
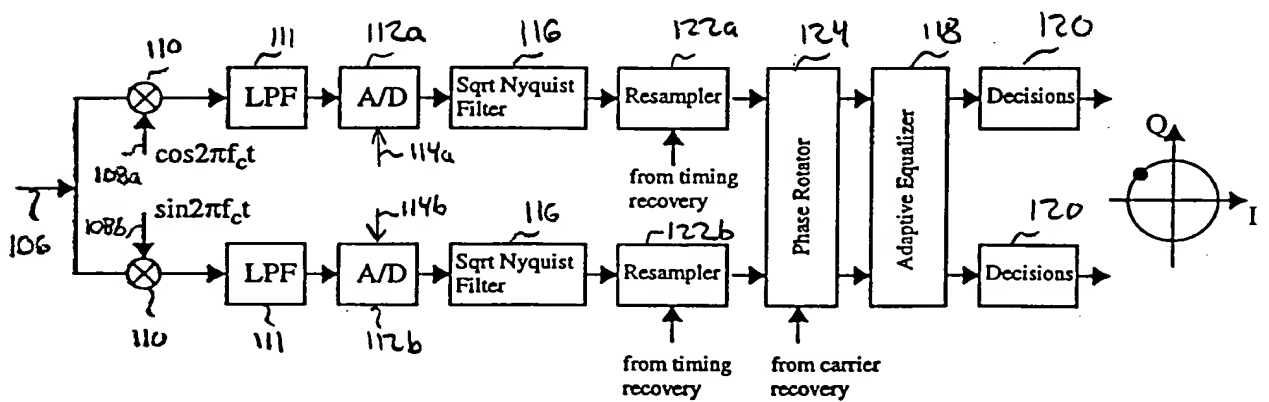


Figure 1c Simplified block diagram of an OFDM system.



**Figure 1D** PSK receiver with carrier and timing recovery.

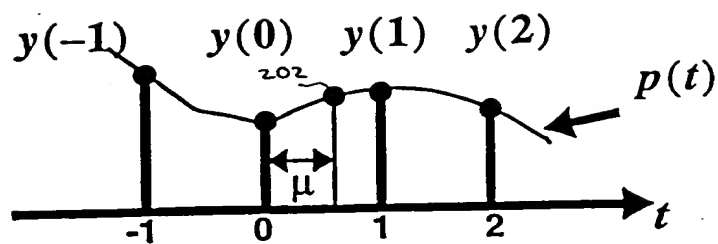


Figure 2 Interpolation Environment

000001 64286960

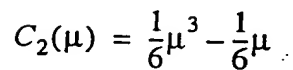
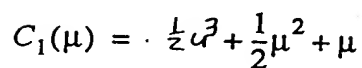
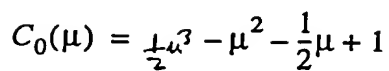
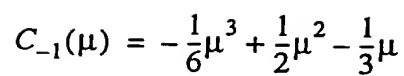


Figure 3 The Lagrange basis polynomials.

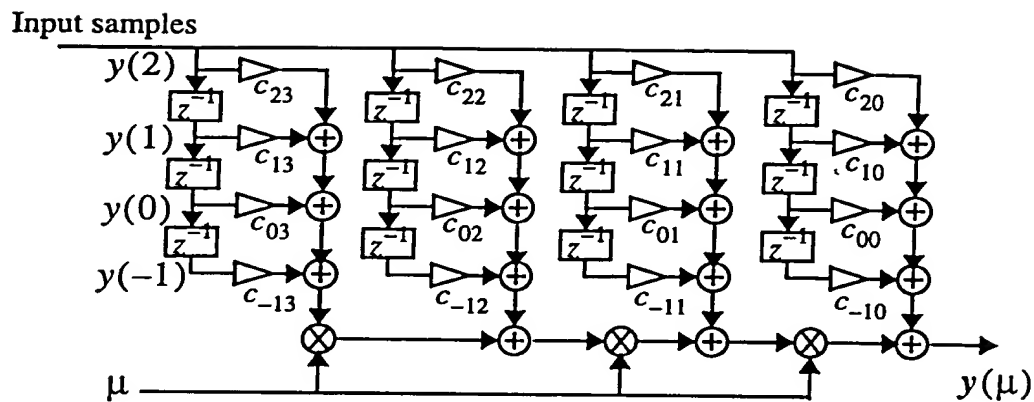


Figure 4 The Farrow structure that implements (2.5) and (2.6).

**060708**

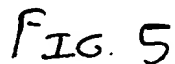


FIG. 6A

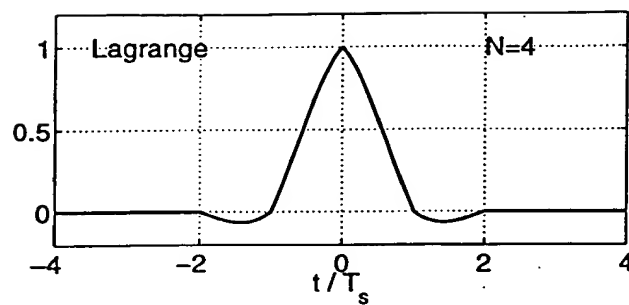


FIG. 6B

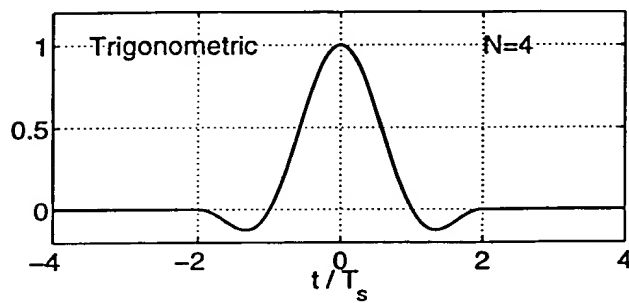


FIG. 6A-6B Impulse responses of (a) Lagrange interpolator and (b) Trigonometric interpolator.

000001 64286960

000001 64286960

FIG. 7A

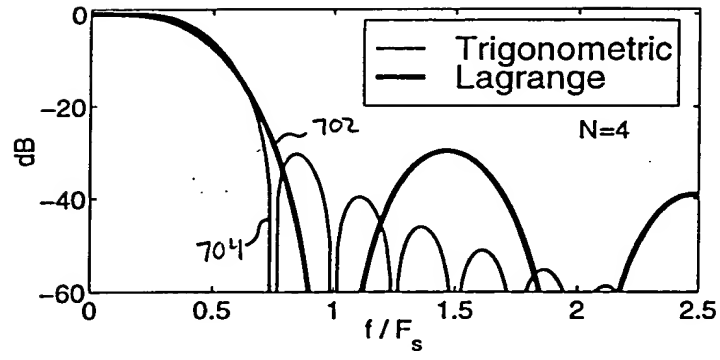


FIG. 7B

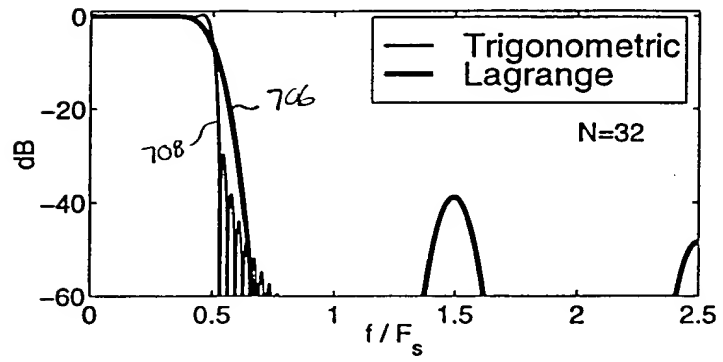


FIG. 7A-7B: Frequency responses for (a)  $N=4$  and (b)  $N=32$ .



000001 64286960

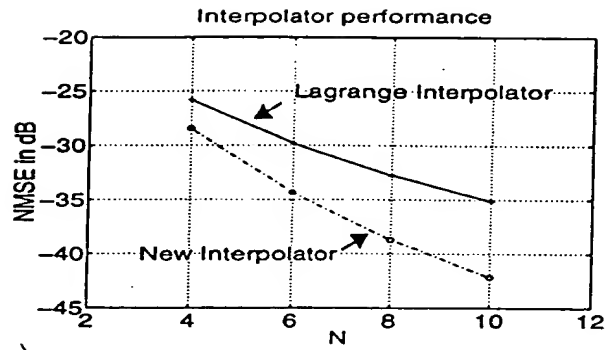


Figure 8B NMSE of the interpolated signal.

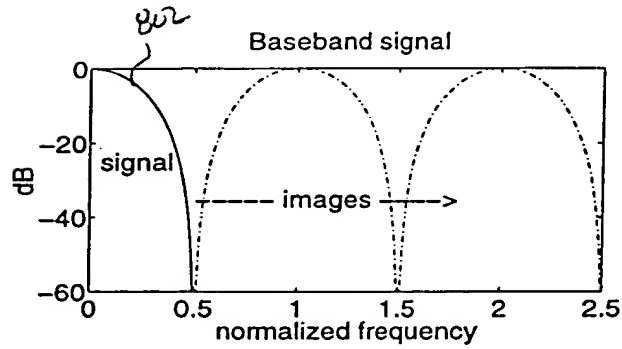


Figure 8A Signal with two samples/symbol and 100% excess BW.

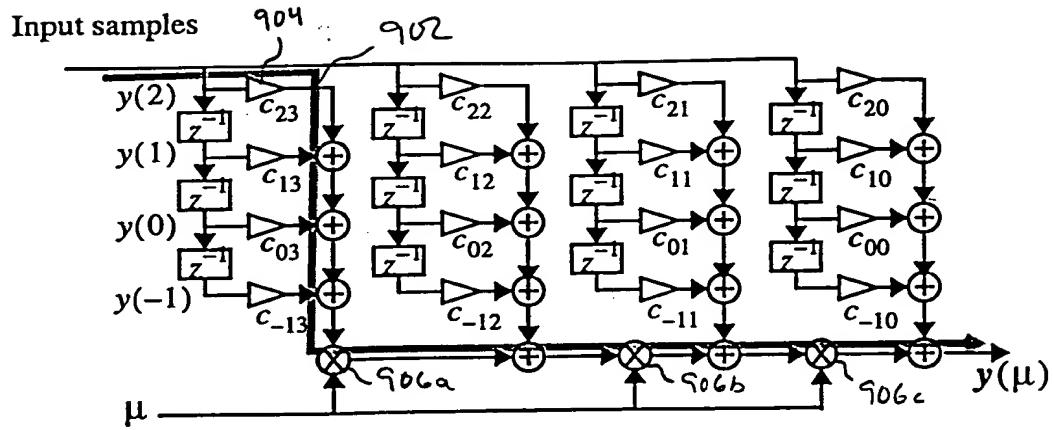


Figure 9 The critical path of the Lagrange cubic interpolator.

1000

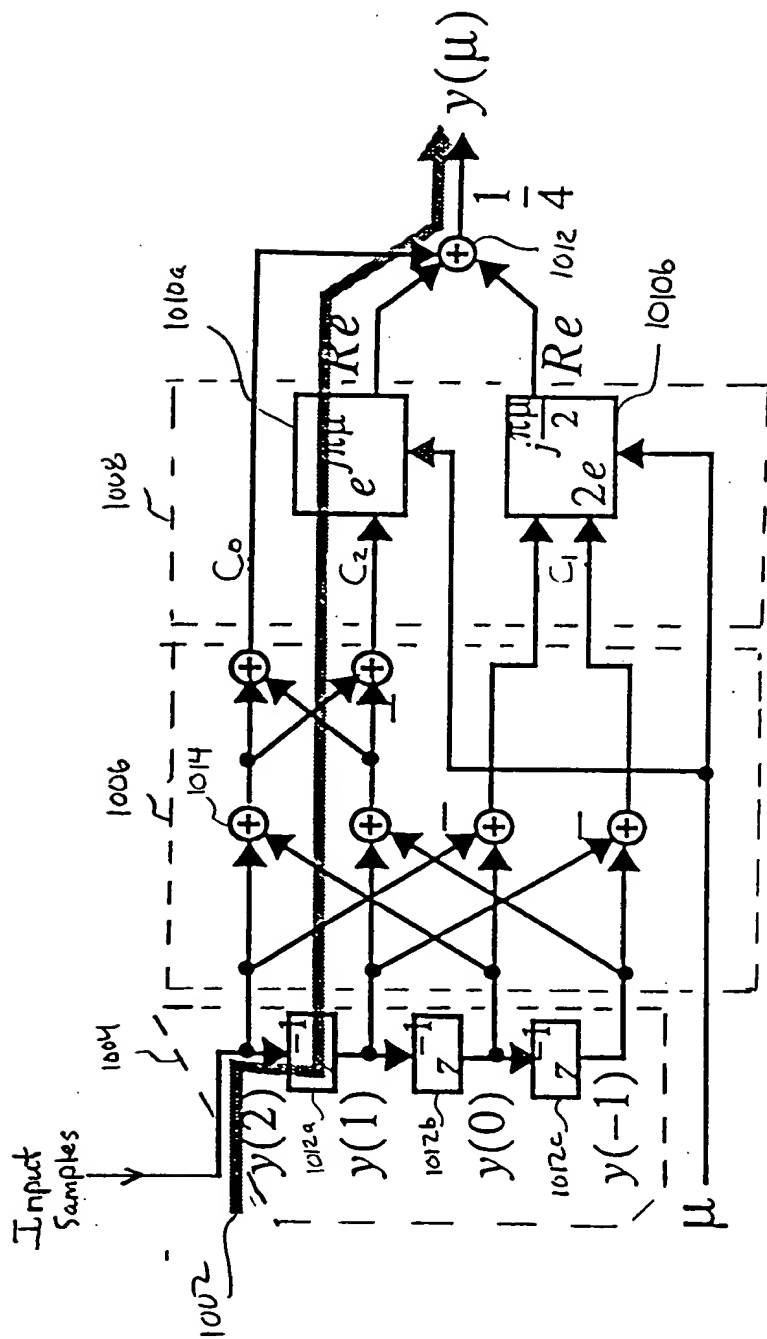


FIG. 10° Trigonometric Interpolator (N=4)

1100

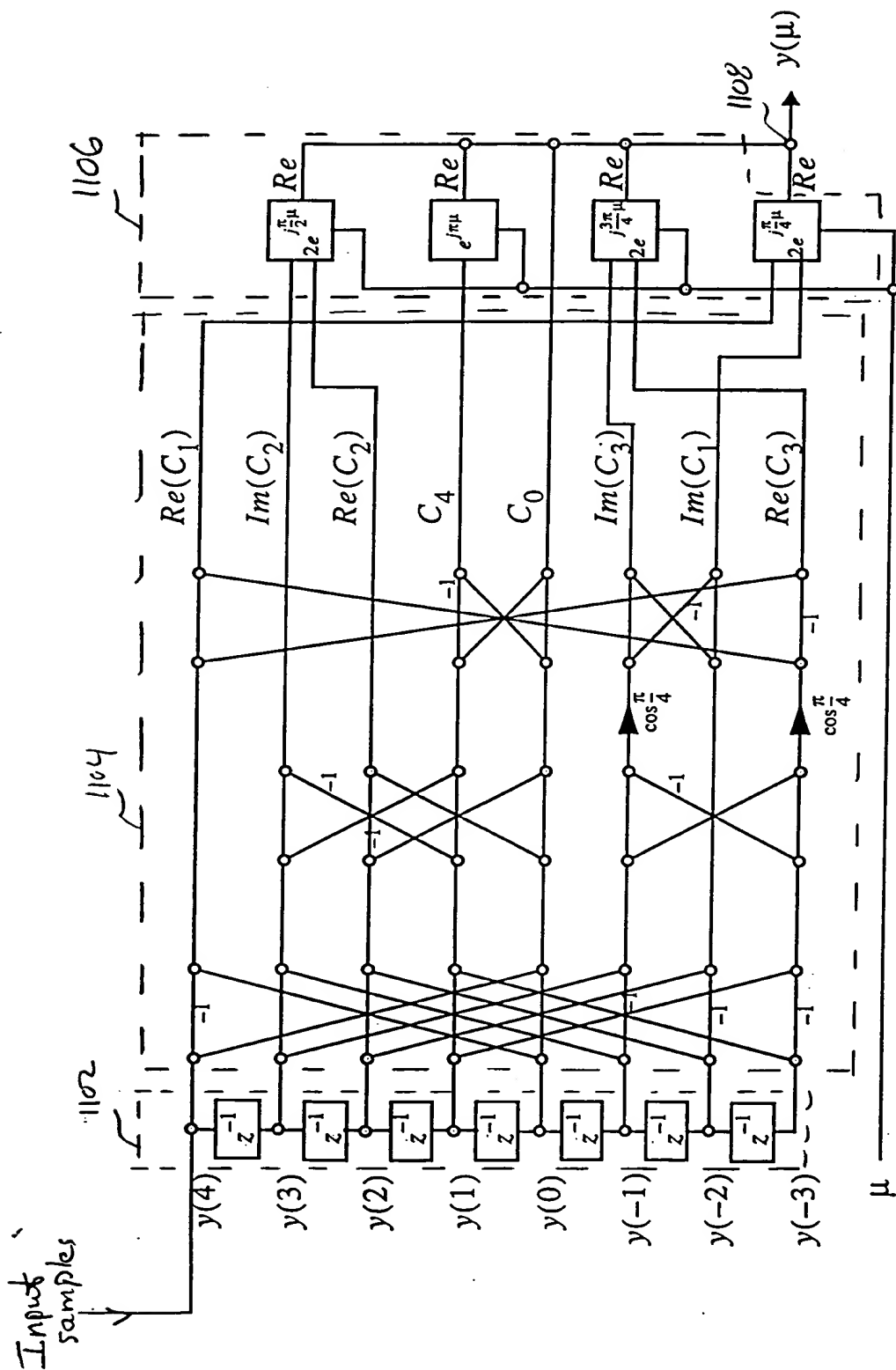


Figure 11 Trigonometric Interpolator with  $N=8$ .

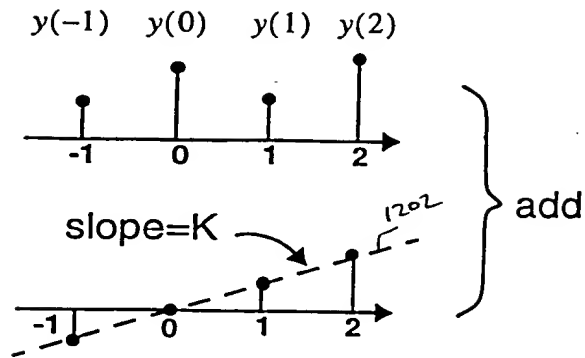


Figure 12 Conceptual modification of input samples.

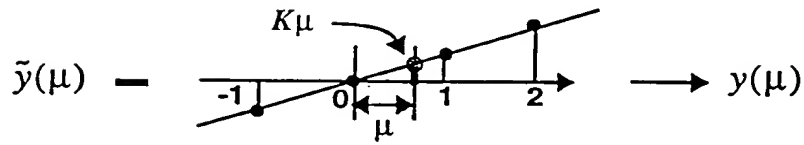


Figure 13 Correcting the offset due to modification of original samples.

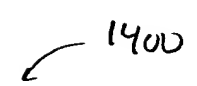


FIG. 14: Trigonometric Interpolator  $N=4$

1500



1506

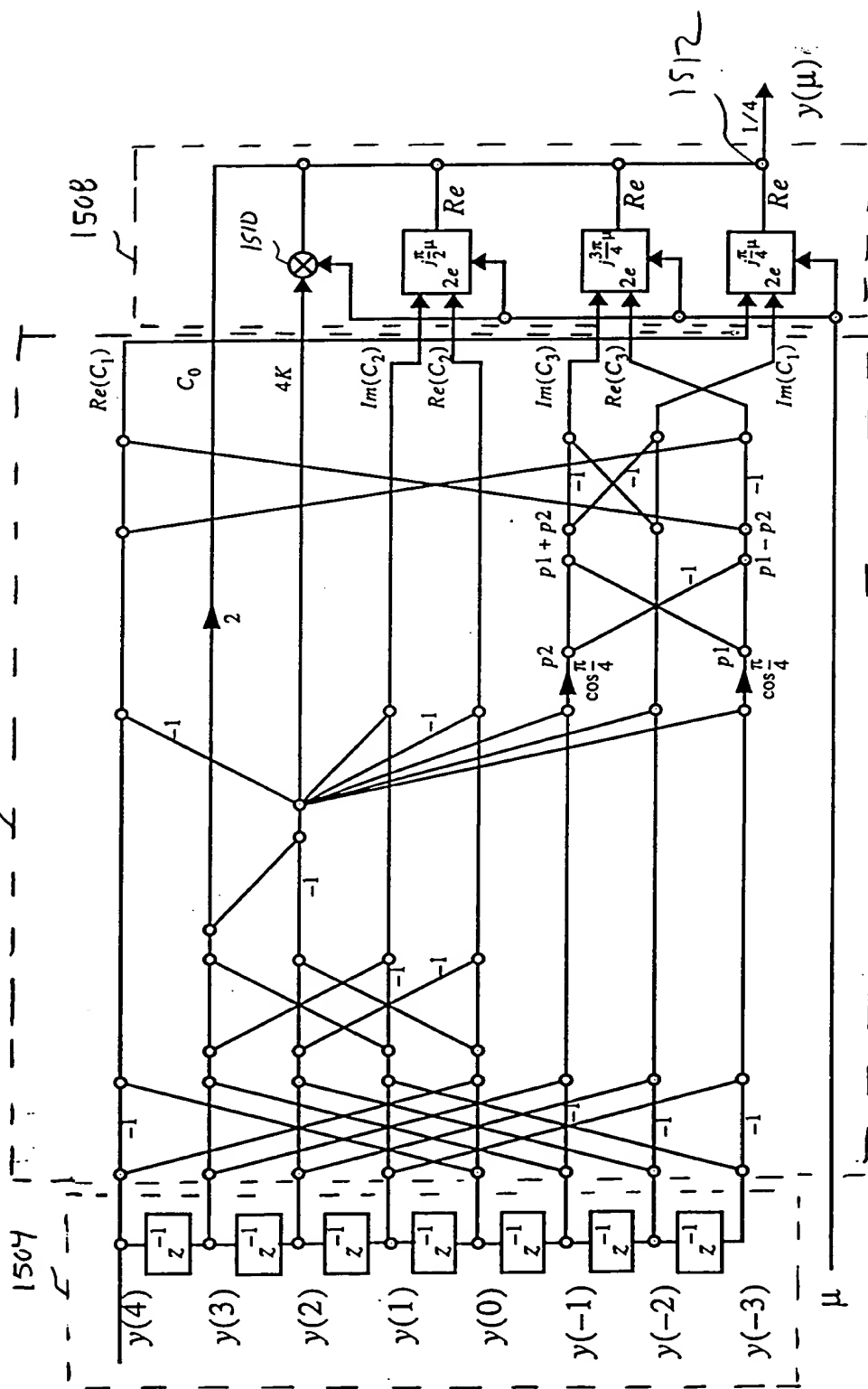


FIG. 15 The modified Trigonometric Interpolator

00000T" 64286960

Interpolation errors are shown in gray.

FIG. 16A: Lagrange cubic

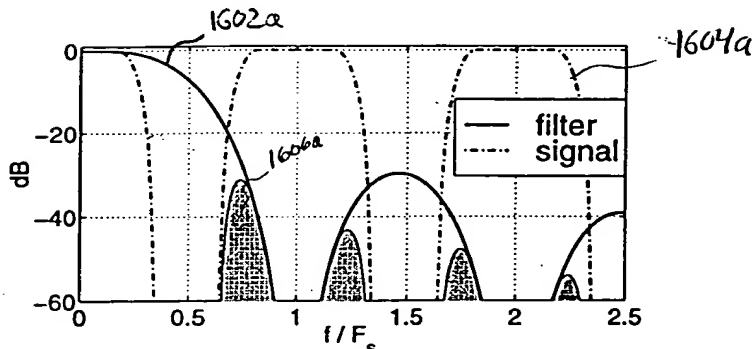


FIG. 16B: Trigonometric Interpolator 1000 (FIG. 10)

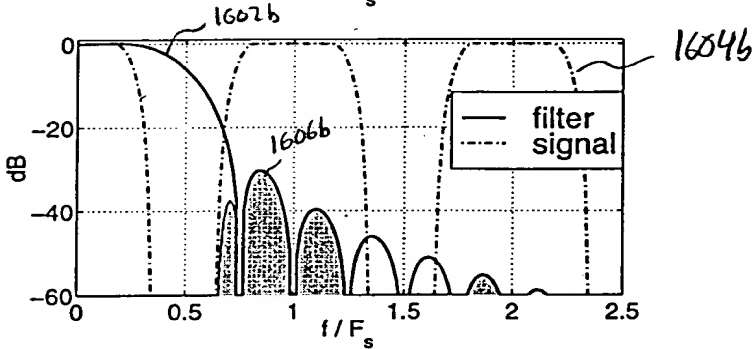


FIG. 16C: Trigonometric Interpolator 1400 (FIG. 14)

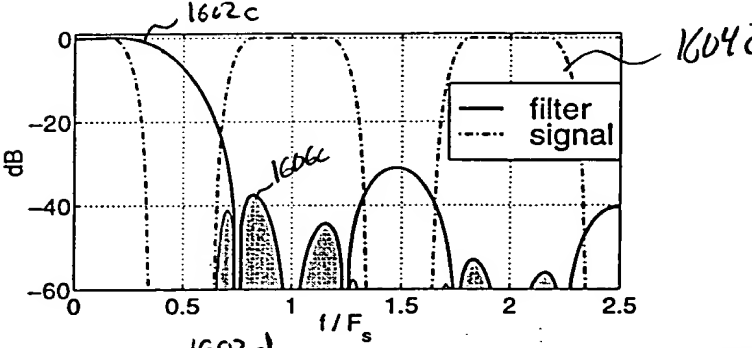
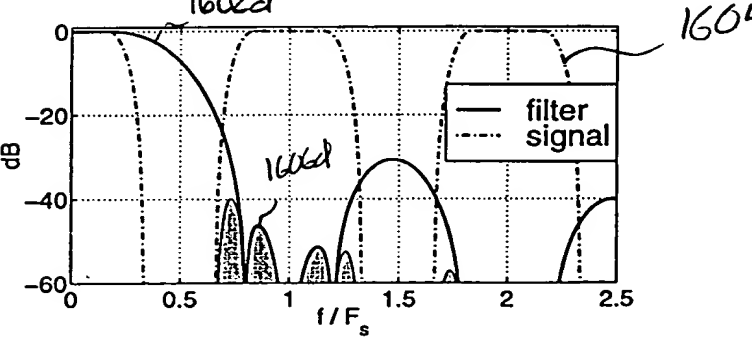


FIG. 16D: Optimal structure





1700

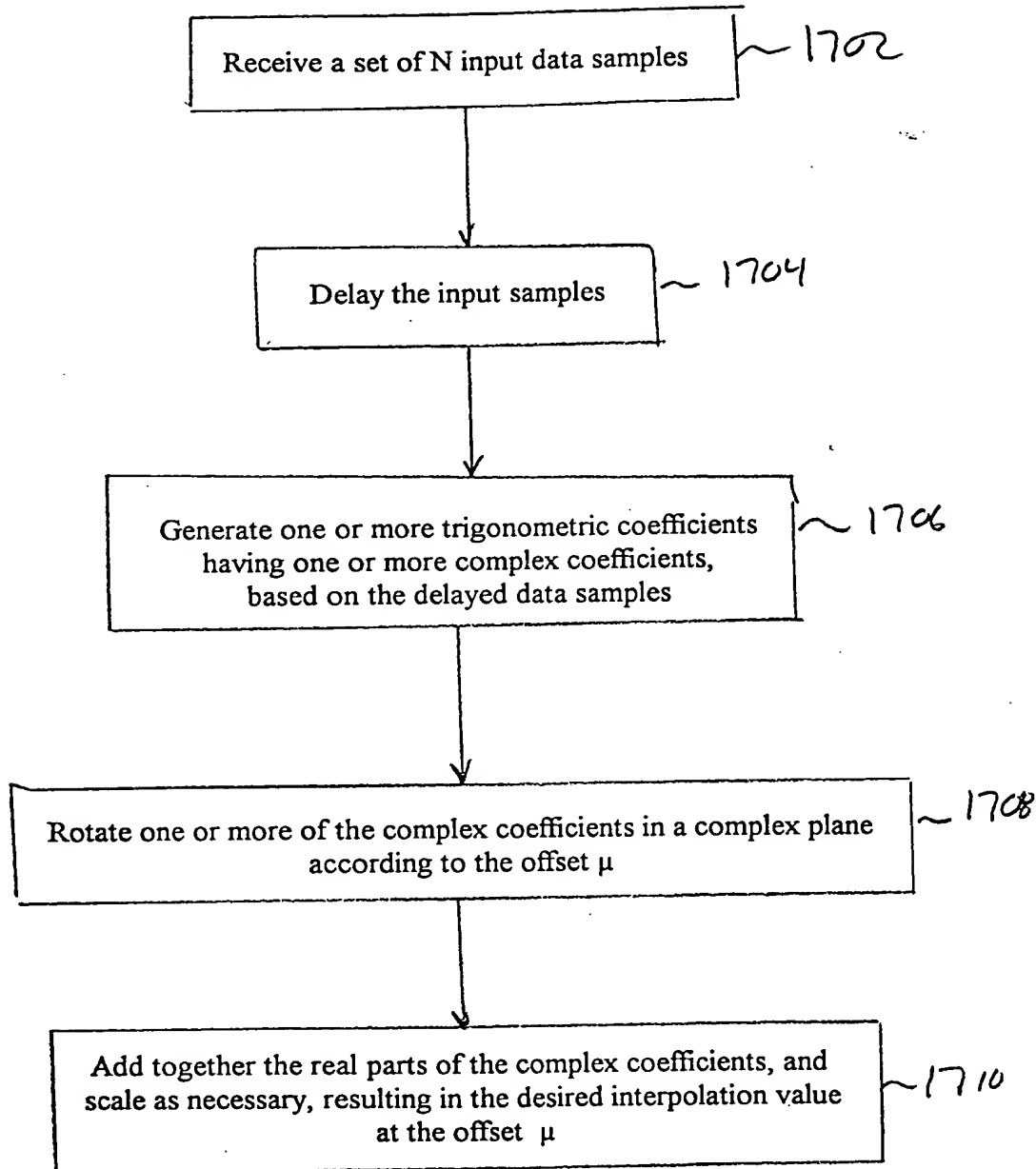
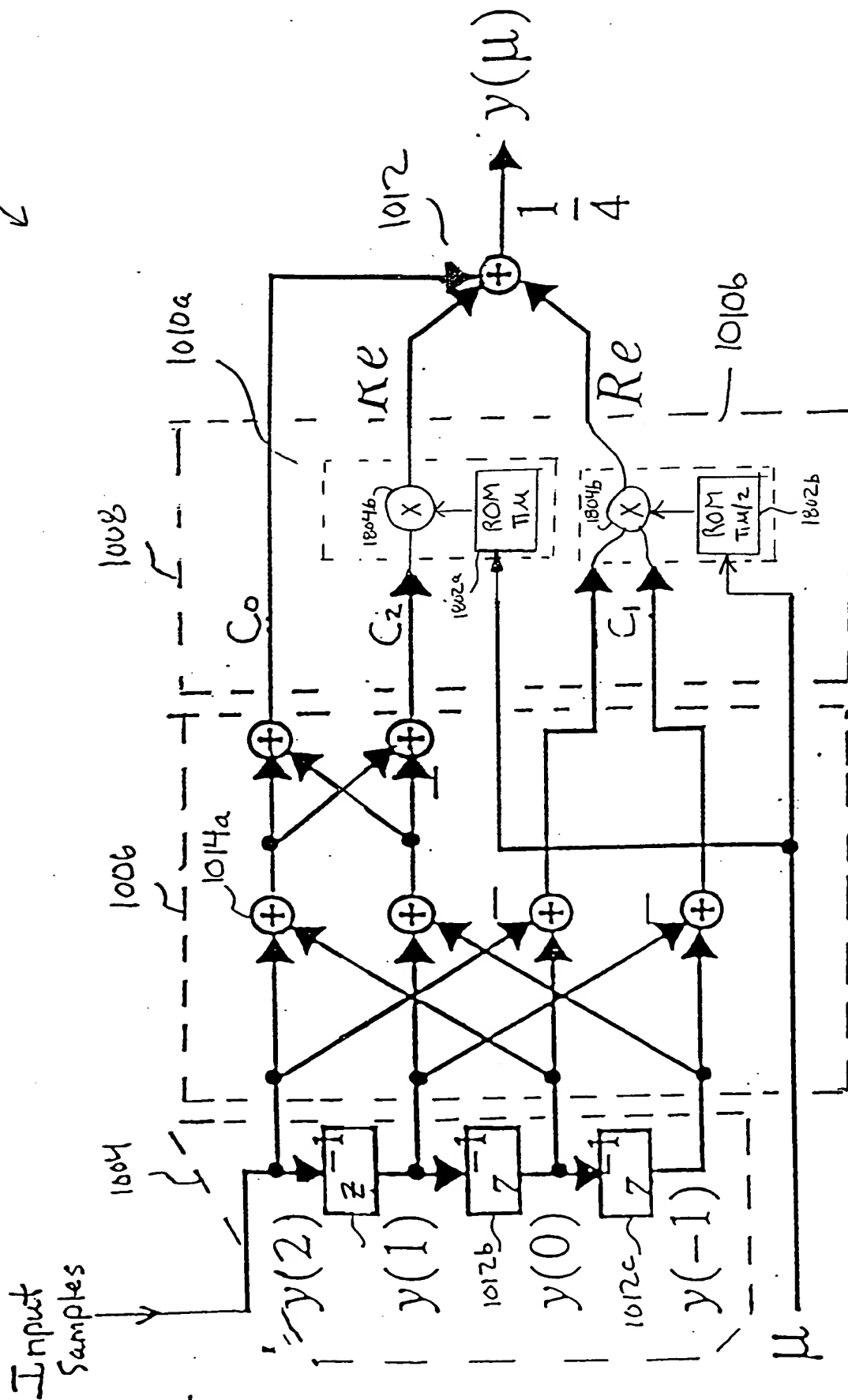


FIG. 17



↓

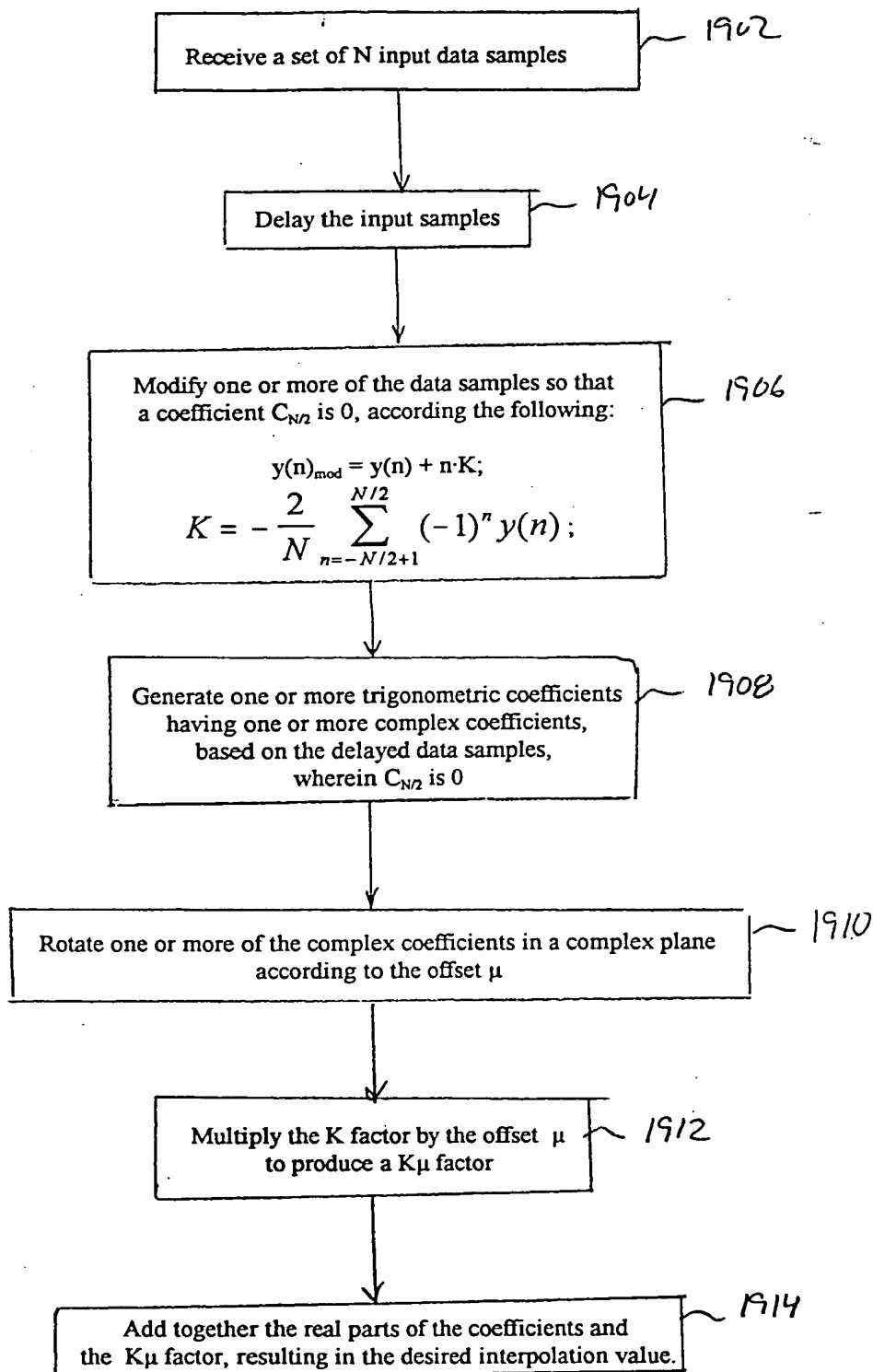


FIG. 19

00000000000000000000000000000000

000001" 64286960

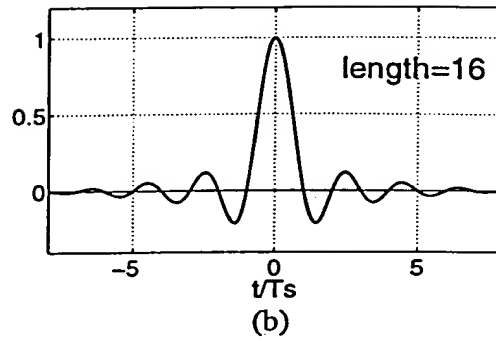
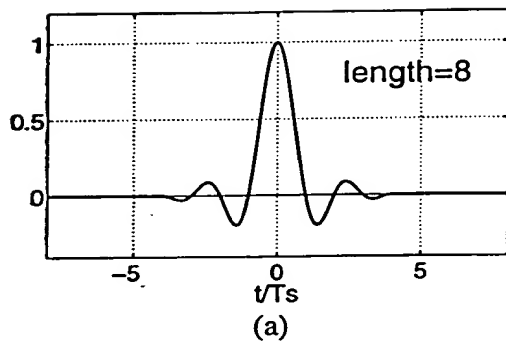


FIG.20: Normalized Impulse responses  $f$  of the interpolation filters.

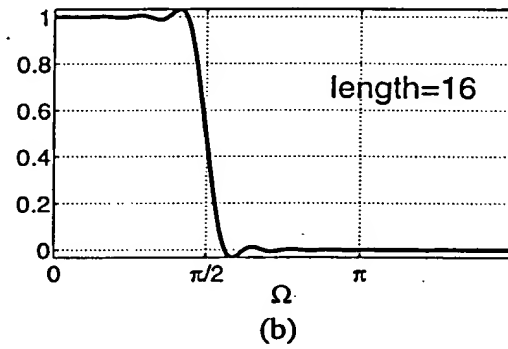
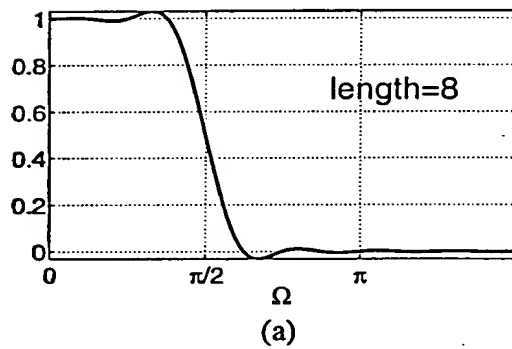


FIG.21: Normalized Frequency responses  $F$  of the interpolation filters.

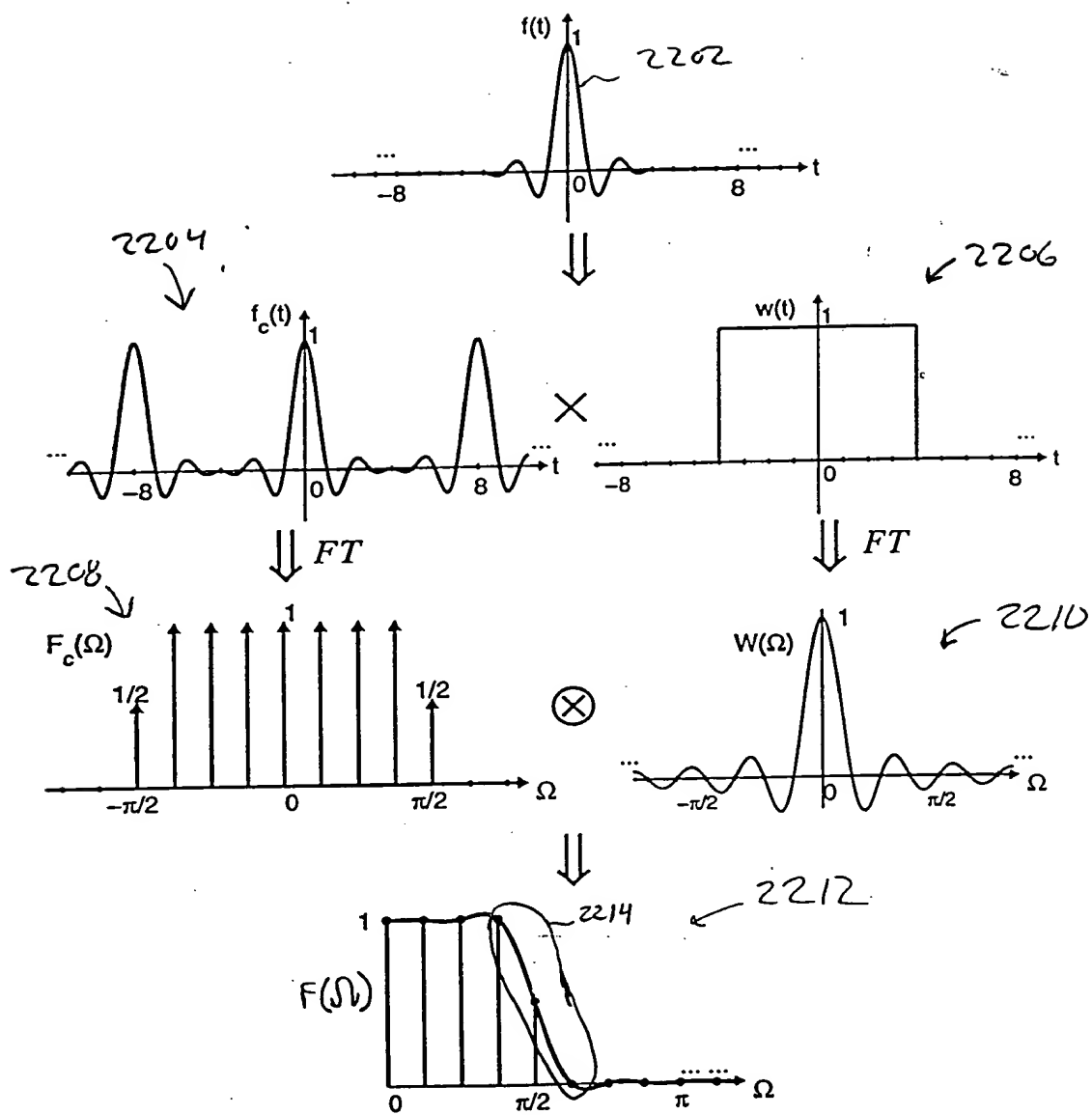


FIG.22 : Analysis of the frequency responses.

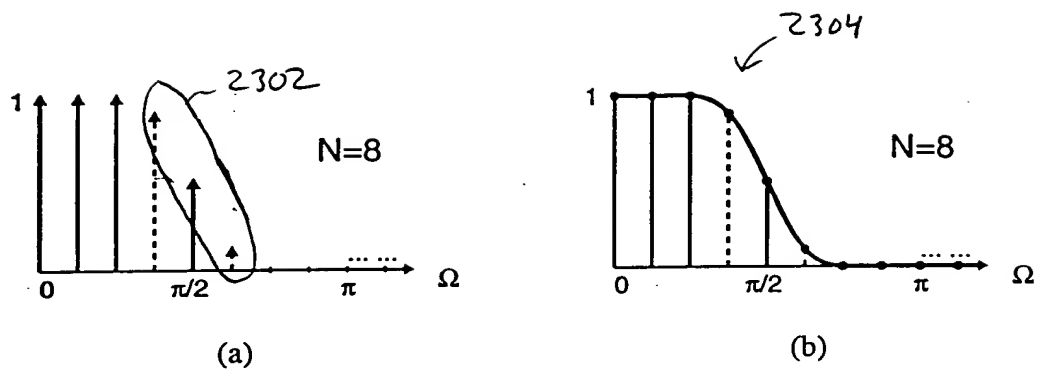


FIG.23 Effect of a more gradual transition at the band edge.

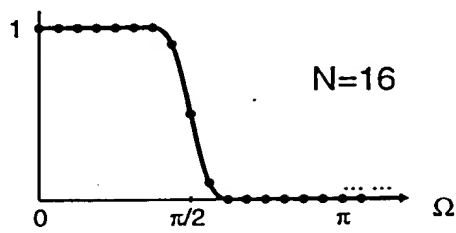


FIG.24 Reducing the transition bandwidth by increasing  $N$ .

3-4b, in which  $N = 8$ .

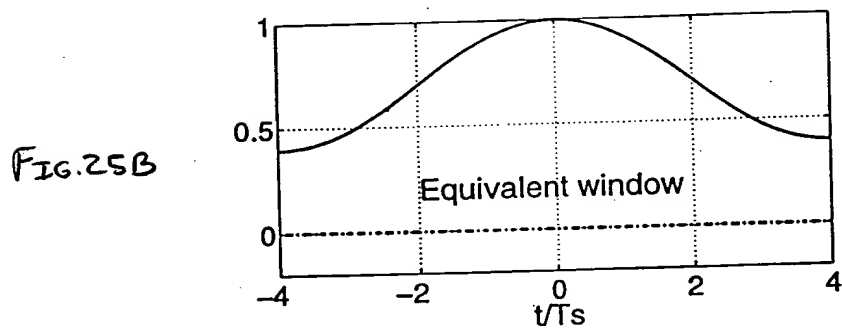
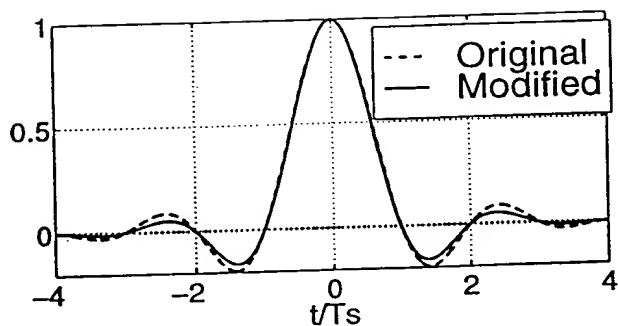


FIG. 25A-B: (A) Impulse response of the original filter and the modified filter: (B) The equivalent window.

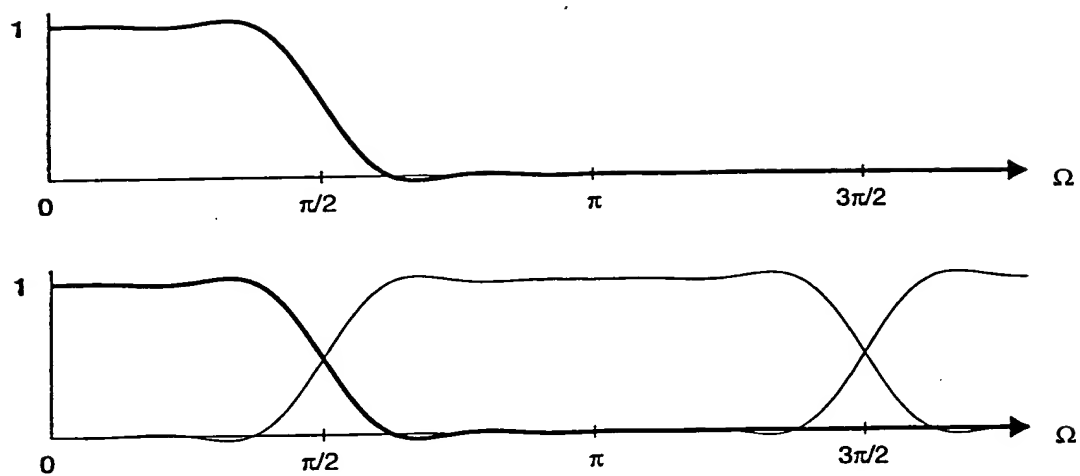


FIG. 26 Forming the frequency response of the discrete-time fractional-delay filter.

000001 64285960



FIG. 27A

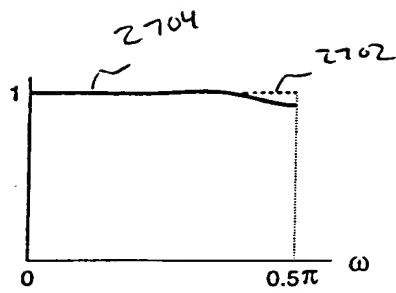


FIG. 27B

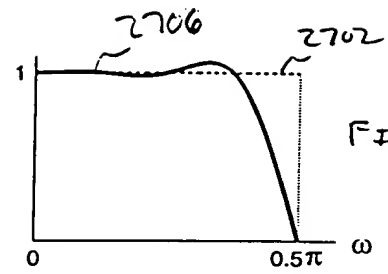


FIG. 27A-B: Fractional-delay filter with (A)  $\mu=0.12$  and (B)  $\mu=0.5$ , using the preliminary  $N=8$  interpolator.

000001 64285960

FIG. 28A

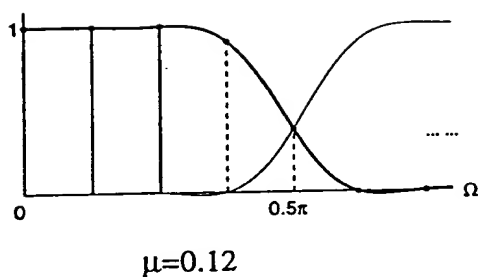


FIG. 28B

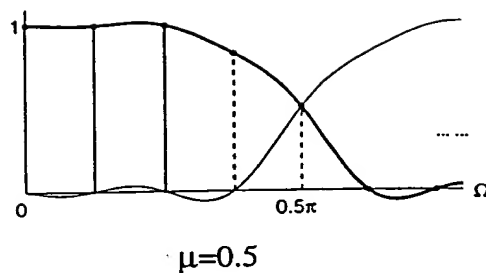


FIG. 28C

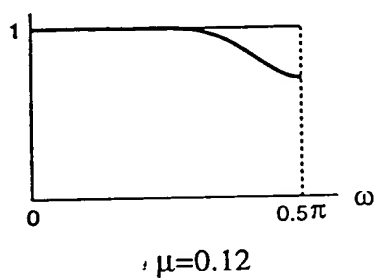
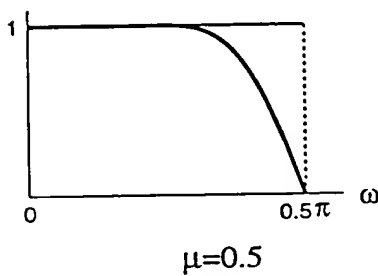


FIG. 28D



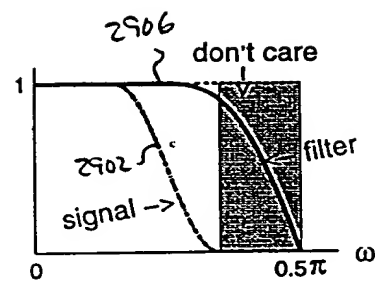
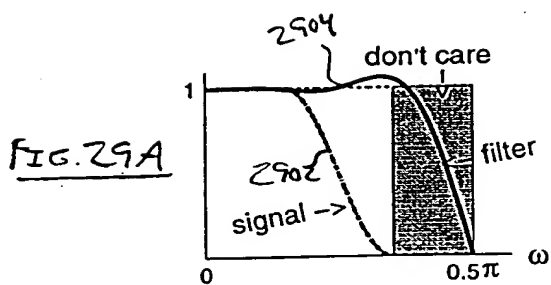


FIG. 29A-B :  $F_{\mu}(\omega)$ , with  $\mu=0.5$ ,  $N=8$ , (A) before and (B) after optimization.

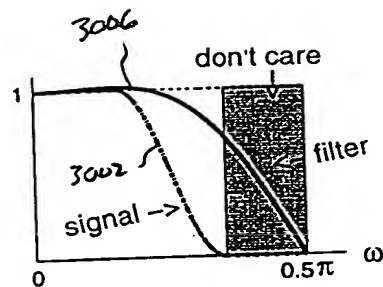
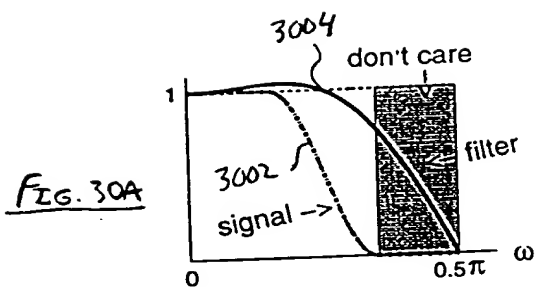


FIG. 30B

FIG. 30A-B  $F_{\mu}(\omega)$  for  $\mu=0.5$ ,  $N=4$ , A) before and B) after modification.

FIG. 31A

3104

1

don't care

filter

3102

signal  $\rightarrow$

0

$0.5\pi \omega$

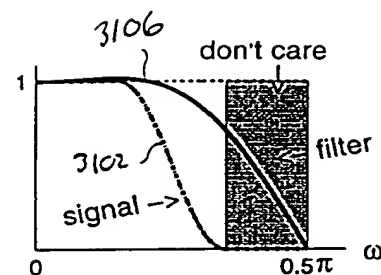


FIG. 3/A-B  $F_{\mu}(\omega)$ ,  $\mu=0.5$ , simplified  $N=4$  structure, A' before and B' after modification.

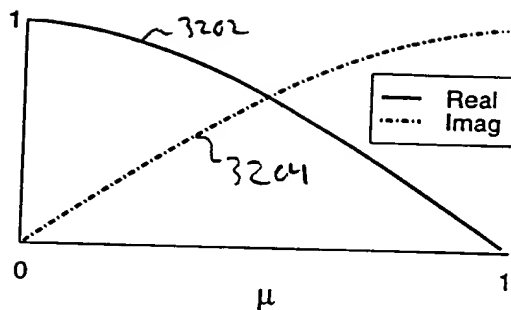


FIG.32: Real and imaginary components of the  $\hat{F}_{\mu}(1)e^{j\frac{\pi}{2}\mu}$  value.

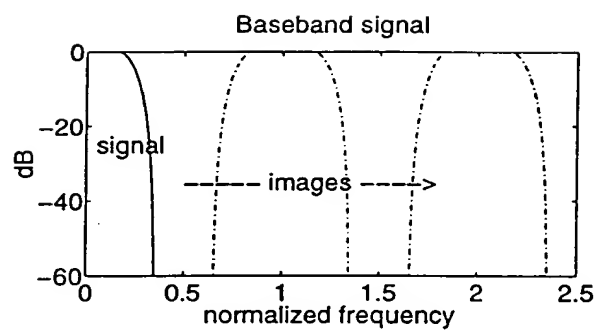


FIG. 33: Signal with two samples/symbol and 40% excess bandwidth.

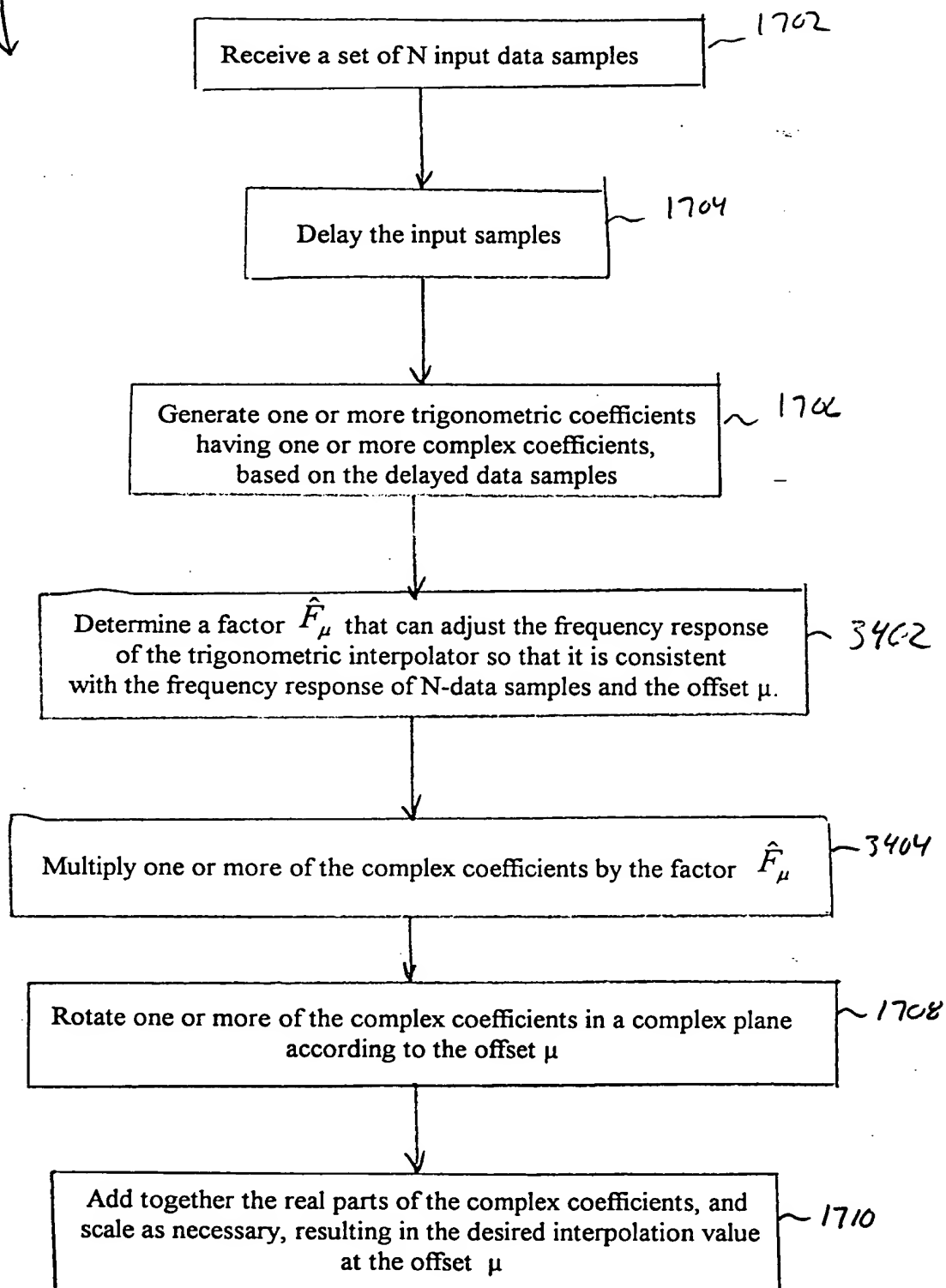


FIG. 34



2009-10-26 14:30



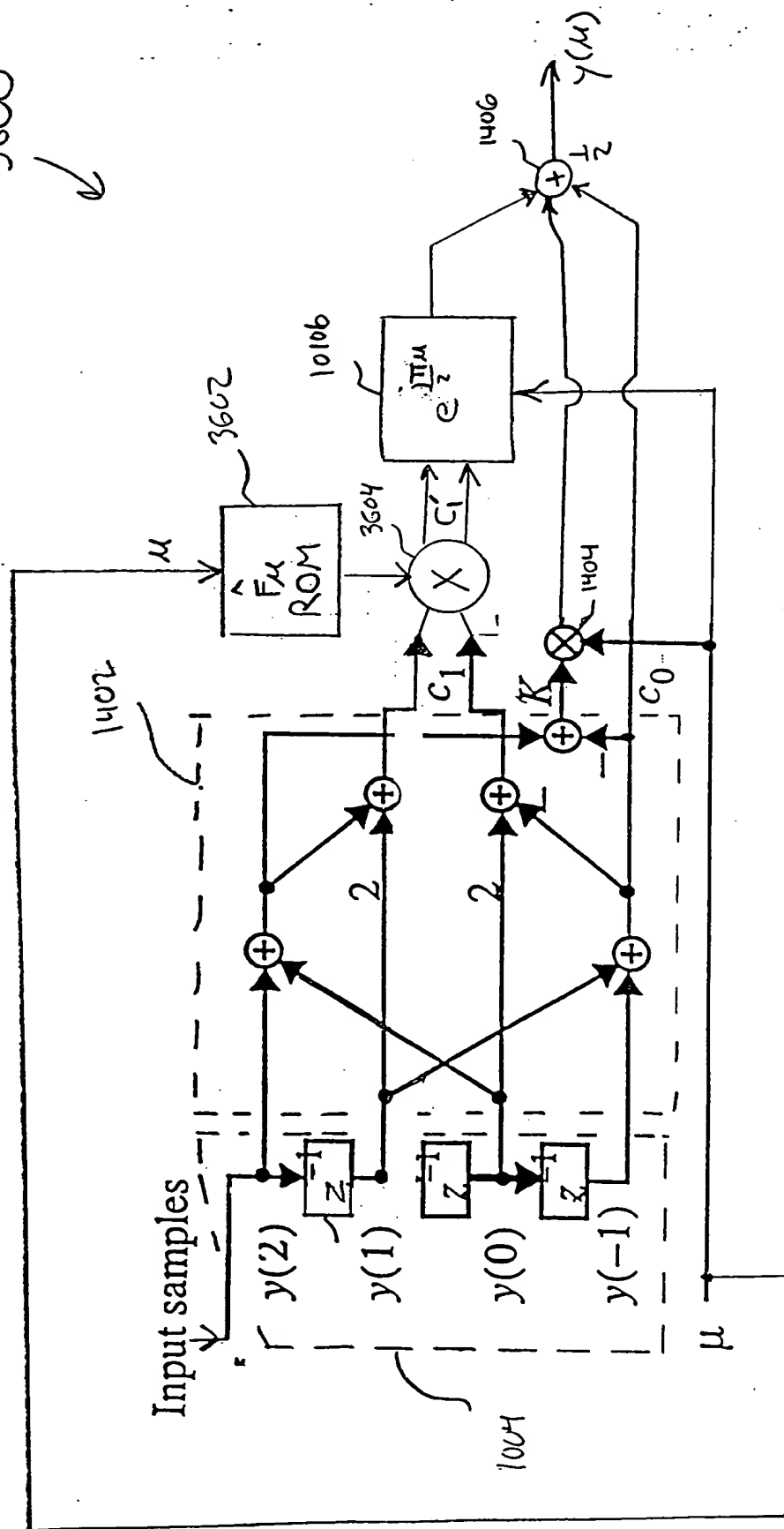


FIG. 36 The *optimized* structure for  $N=4$ .

3700

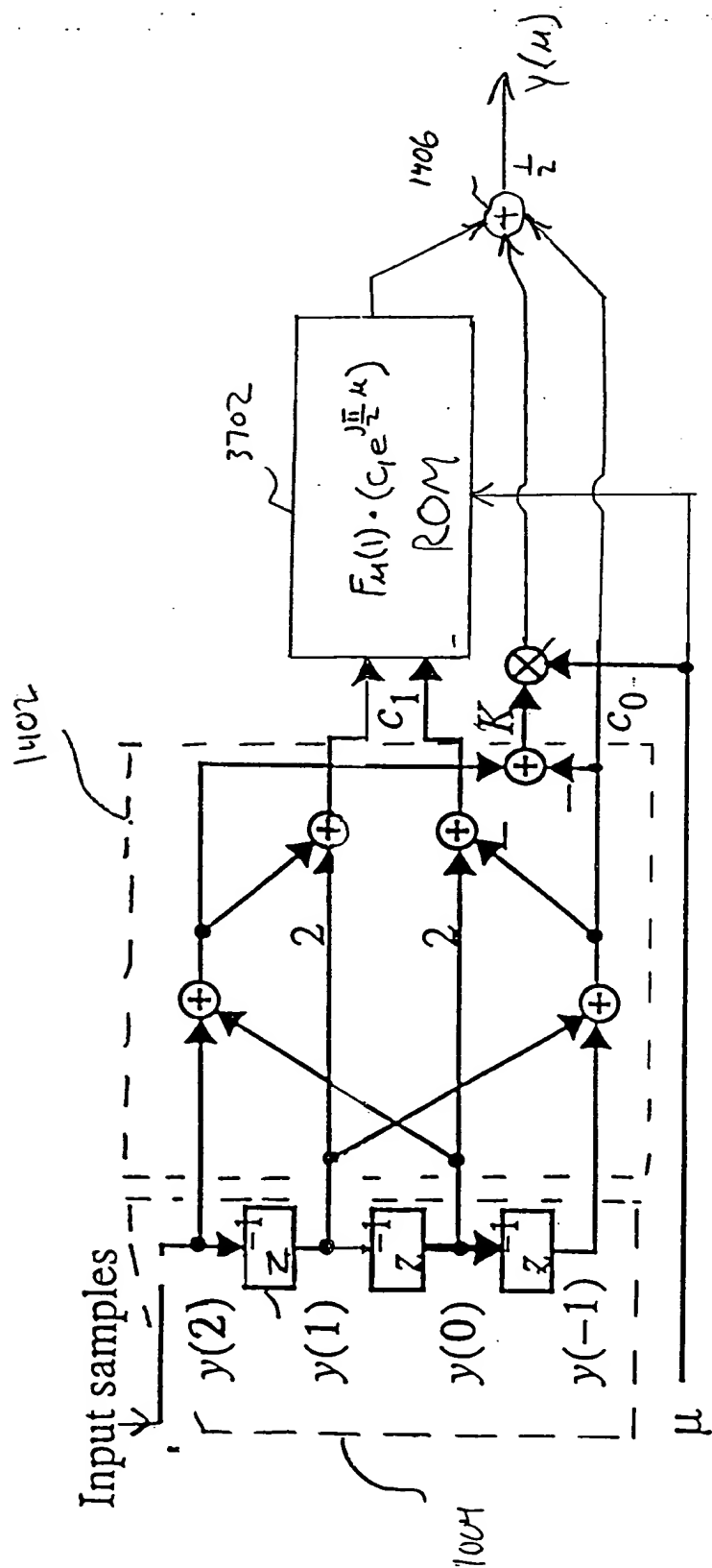


FIG. 37: The optimized structure for  $N=4$ .

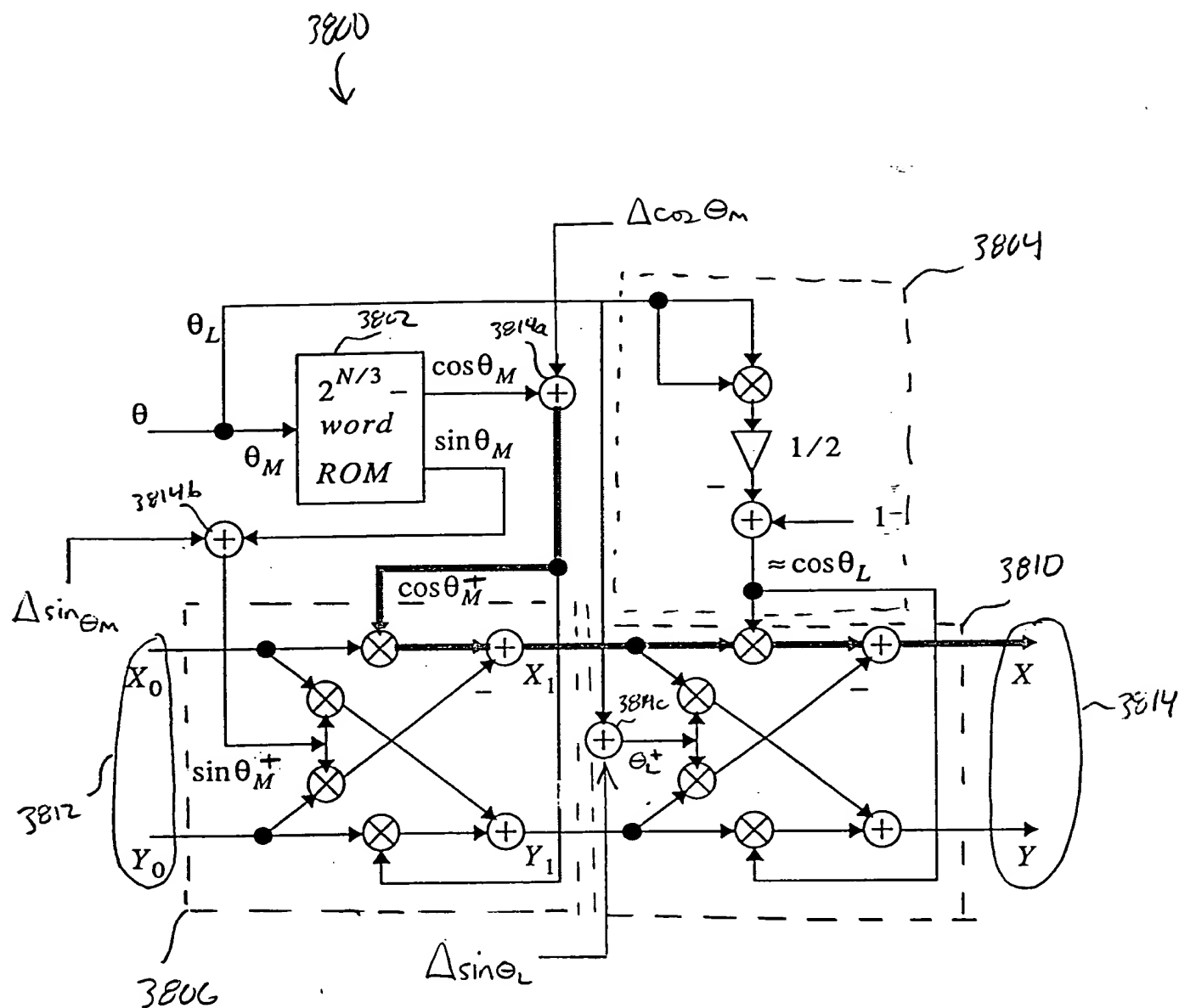


FIG. 38

3906

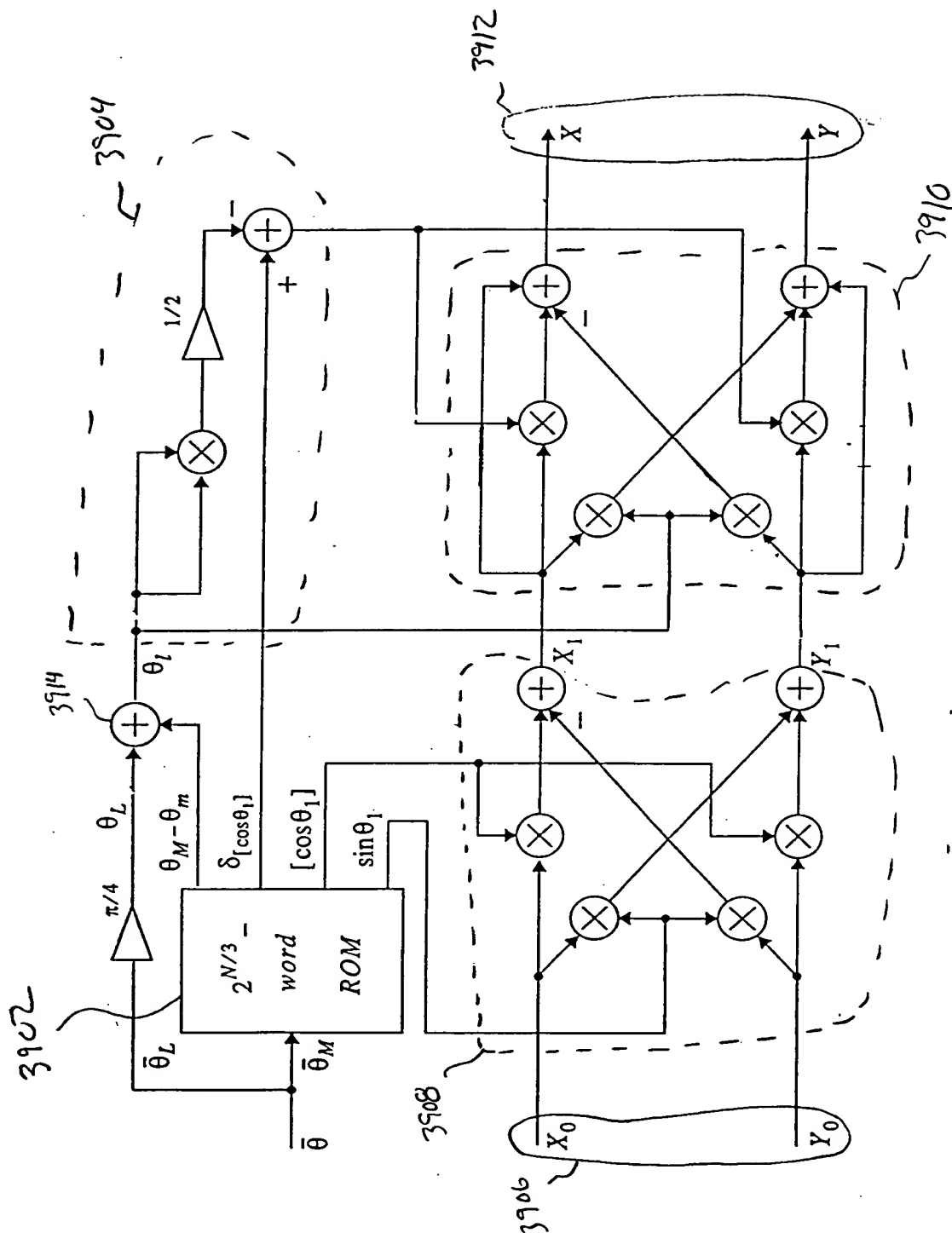


FIG. 39

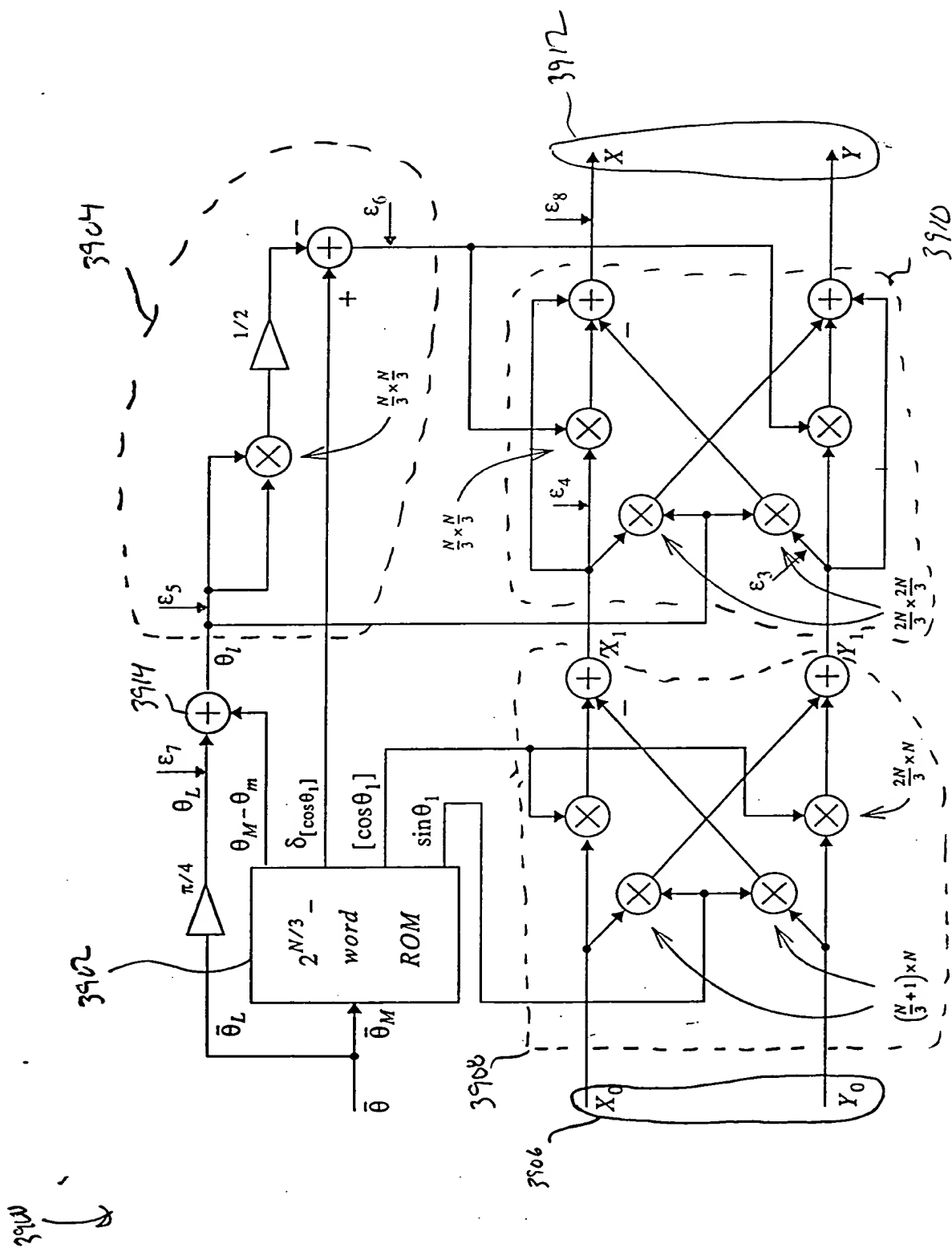


FIG. 40

4100  
↓

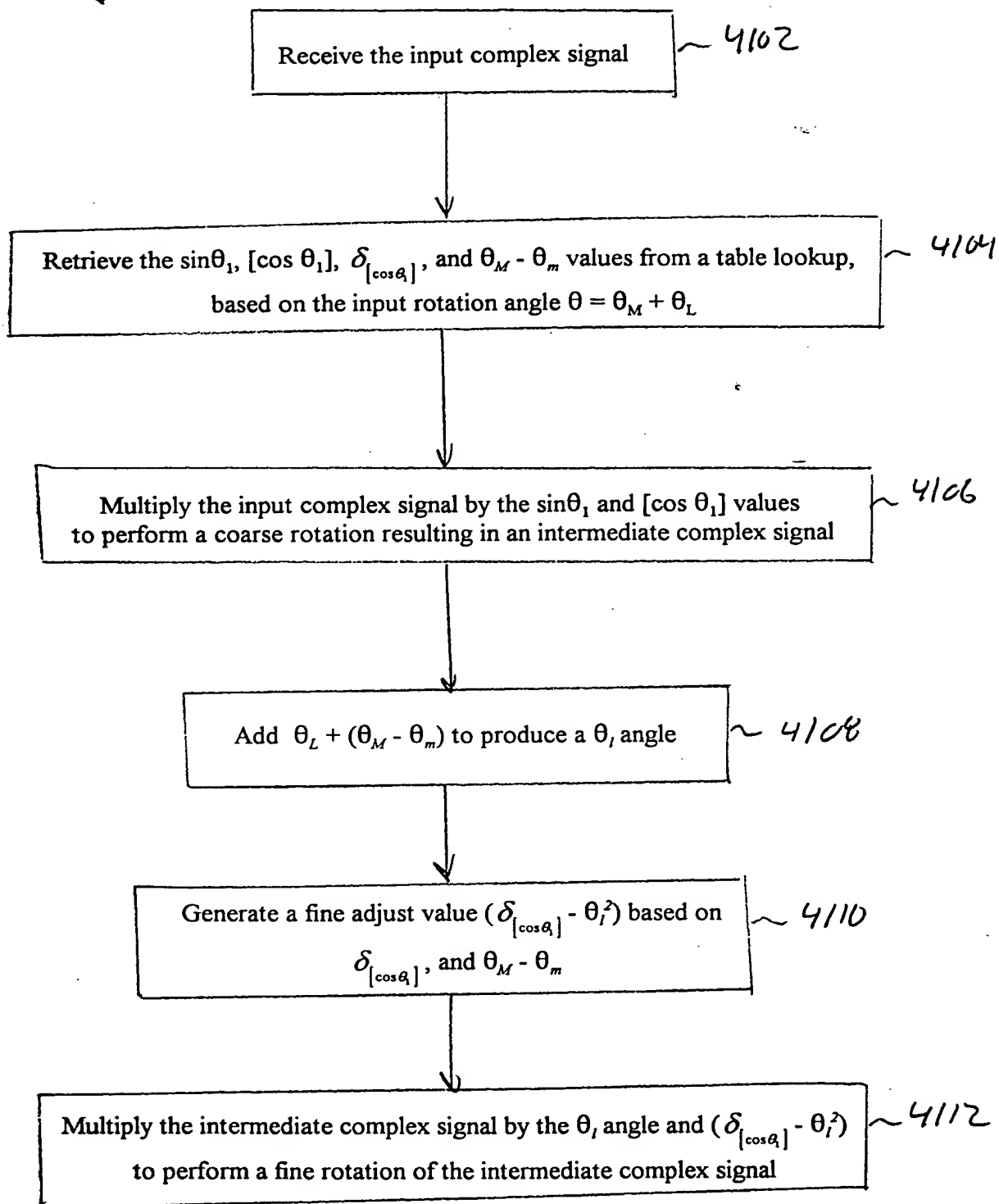


FIG. 41

000001" 64286960

3910  
↓

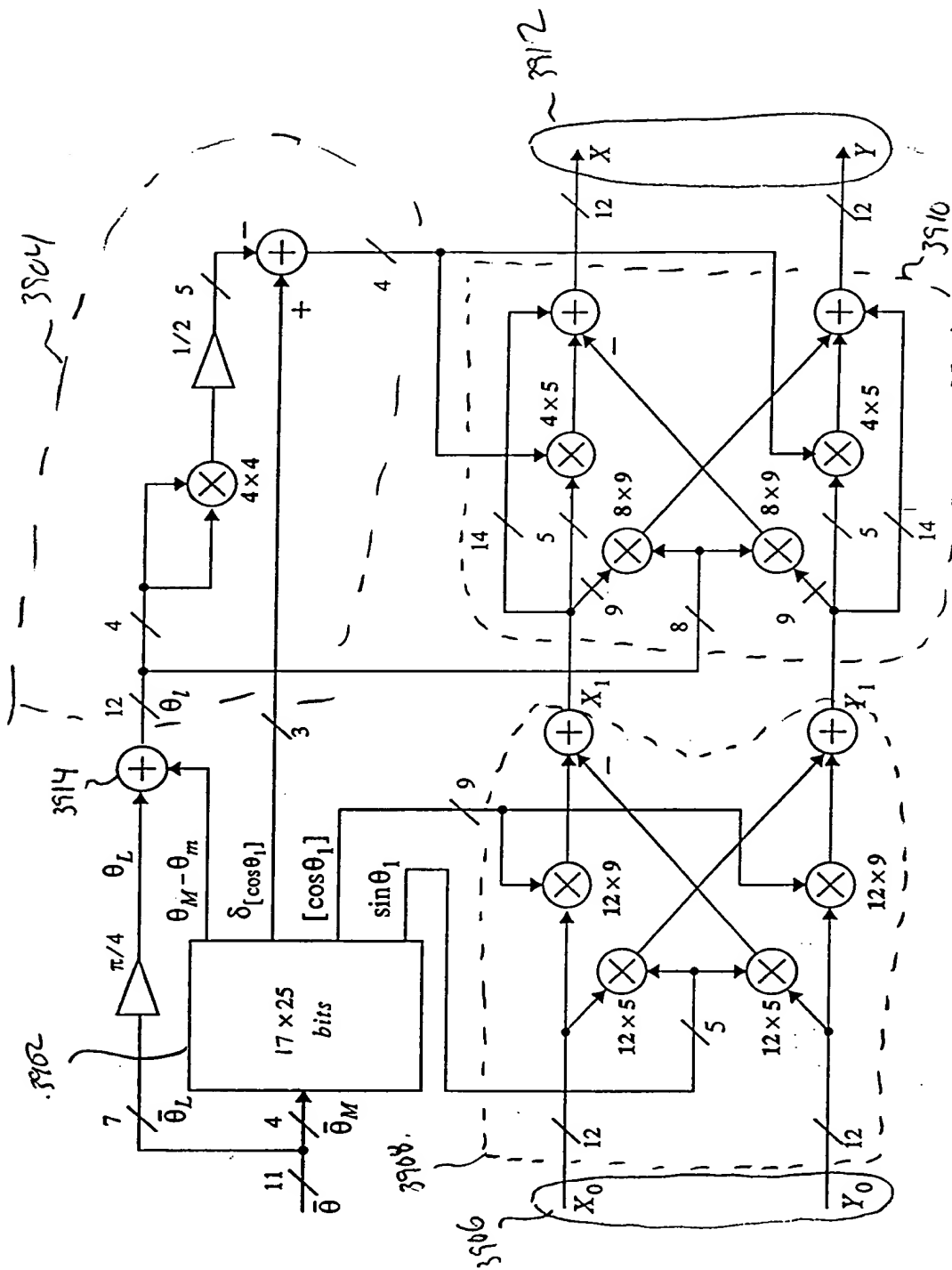


FIG. 42 The internal wordlength of the structure that achieved 90.36 dB SFDR.



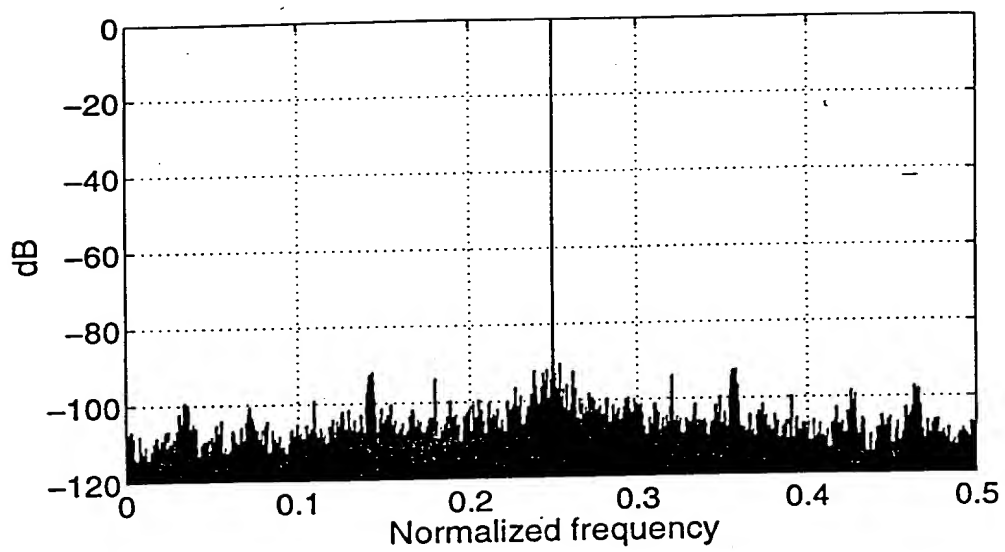


FIG.43 Output spectrum showing 90.36 dB SFDR.

4406

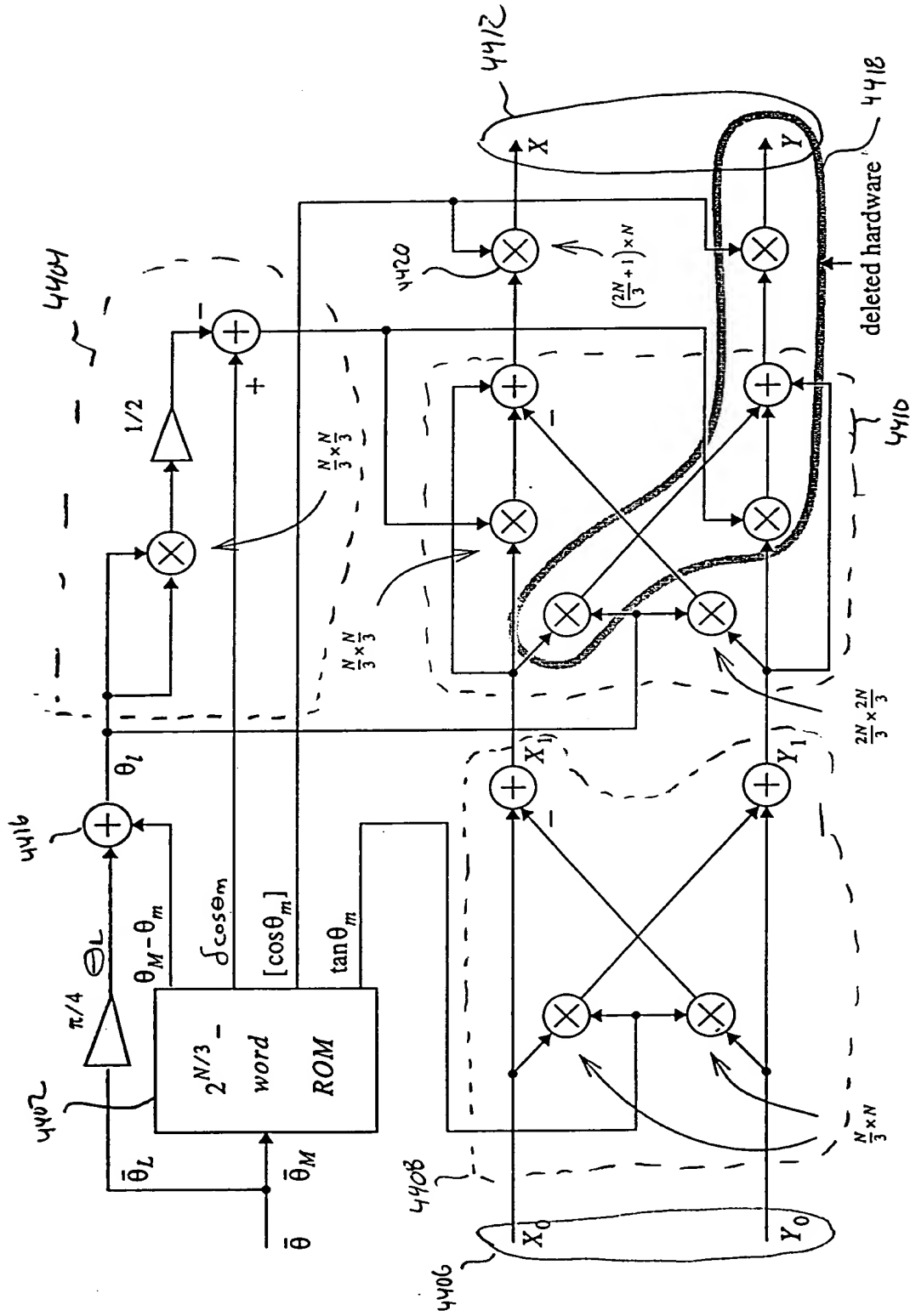


FIG. 44 A modified architecture when only one output is needed.

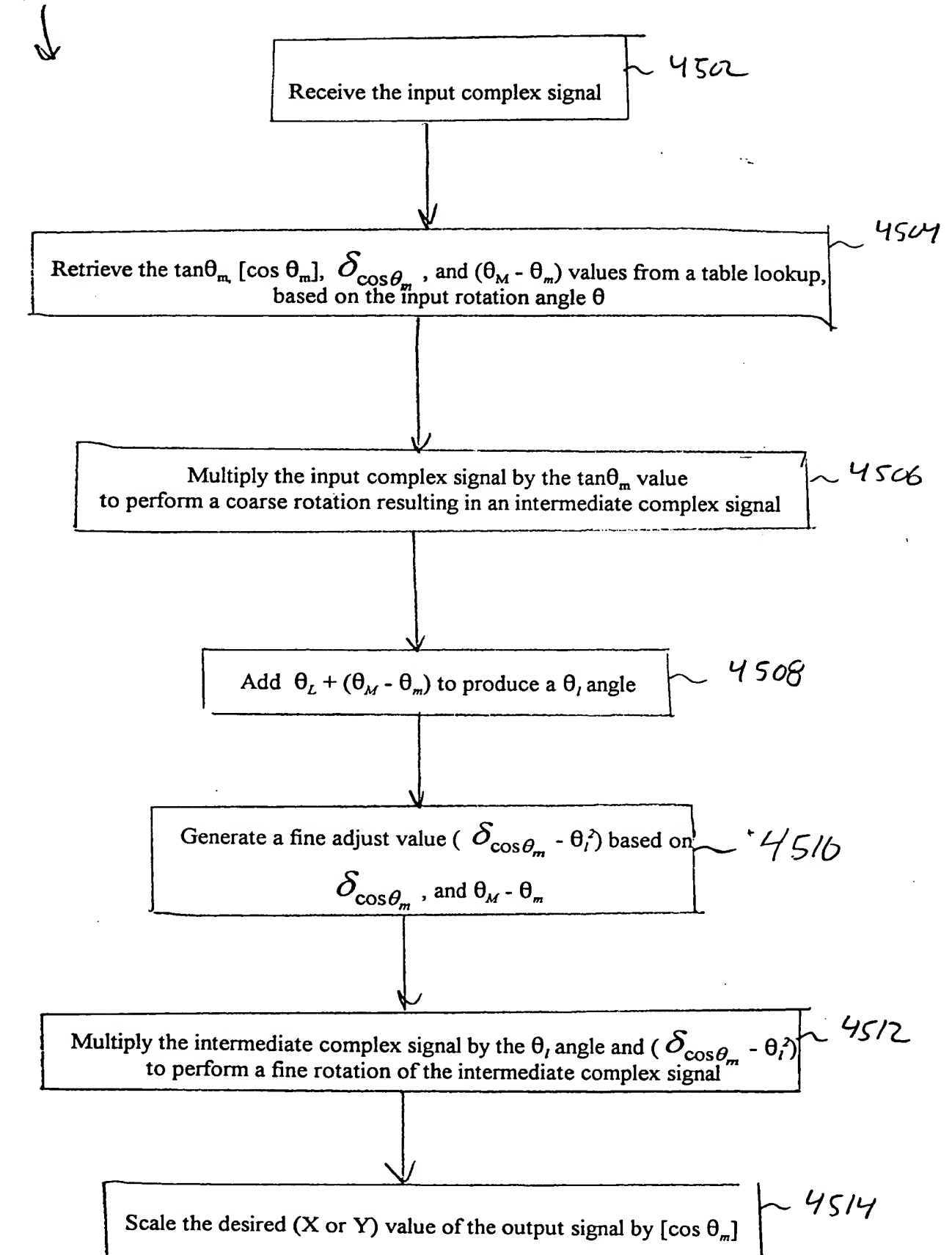


FIG. 45

where the adder is an overflowing accumulator.

4700 →

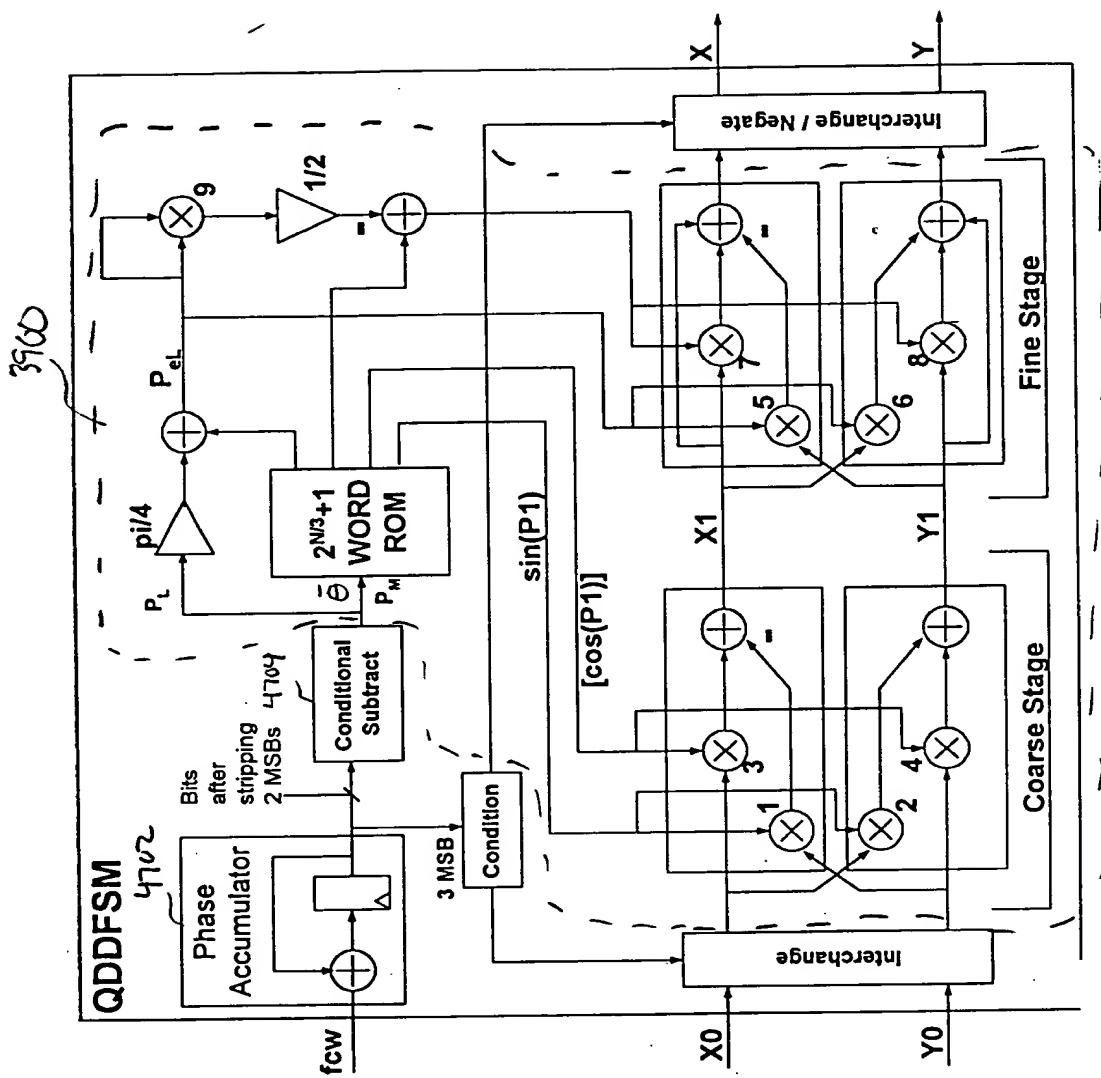


FIG 47

yes →

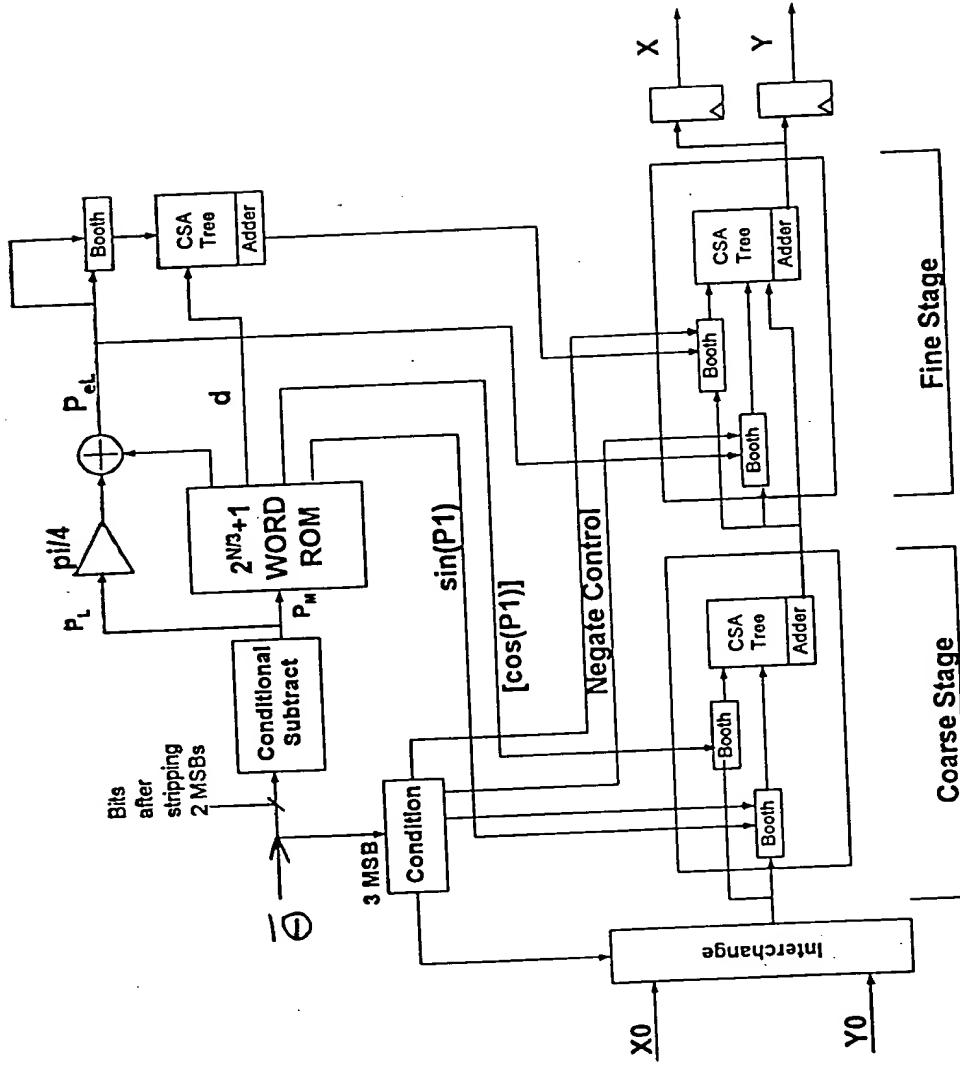


Fig. 48

000001" 64286960

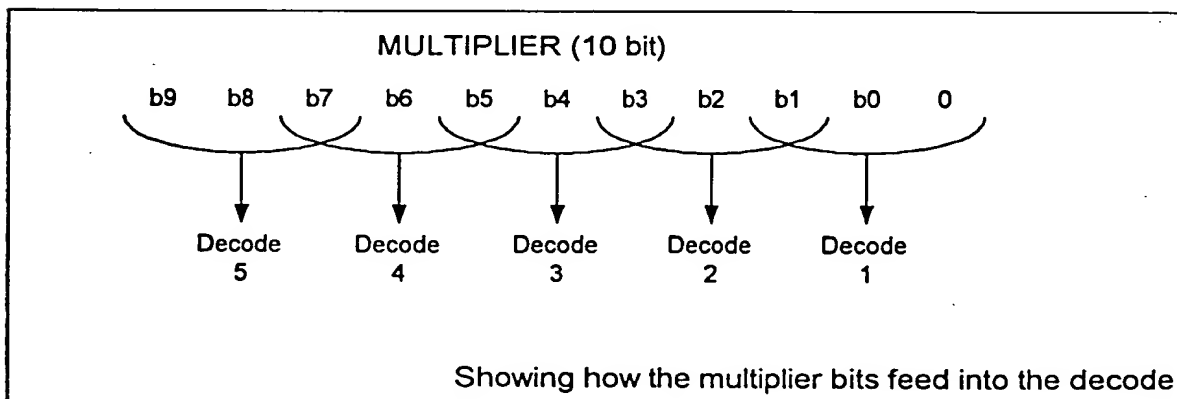
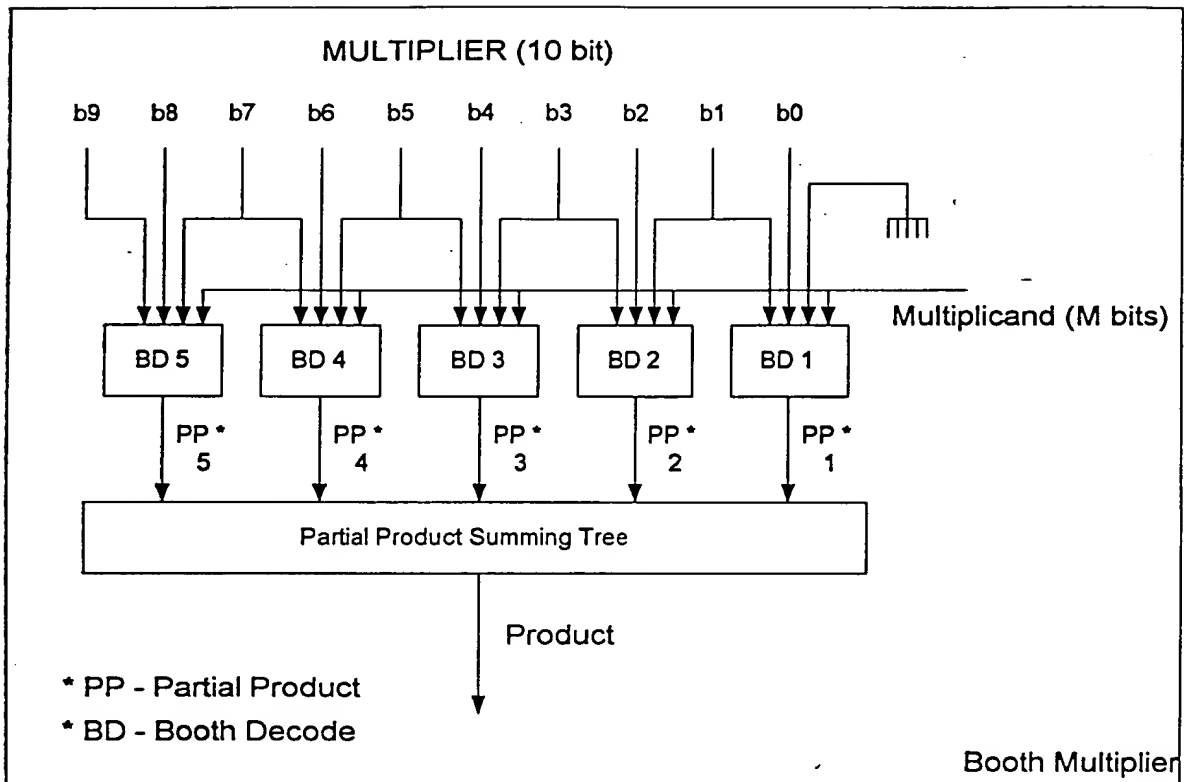


FIG. 49

5000  
↓

Original Booth Table

5002  
↙

b2    b1    b0    PP

0	0	0	0*A
0	0	1	1*A
0	1	0	1*A
0	1	1	2*A
1	0	0	-2*A
1	0	1	-1*A
1	1	0	-1*A
1	1	1	0*A

FIG. 50

5100  
↙

Negating Booth Table

5102  
↙

b2    b1    b0    PP

0	0	0	0*A
0	0	1	-1*A
0	1	0	-1*A
0	1	1	-2*A
1	0	0	2*A
1	0	1	1*A
1	1	0	1*A
1	1	1	0*A

FIG. 51



5260  
↓

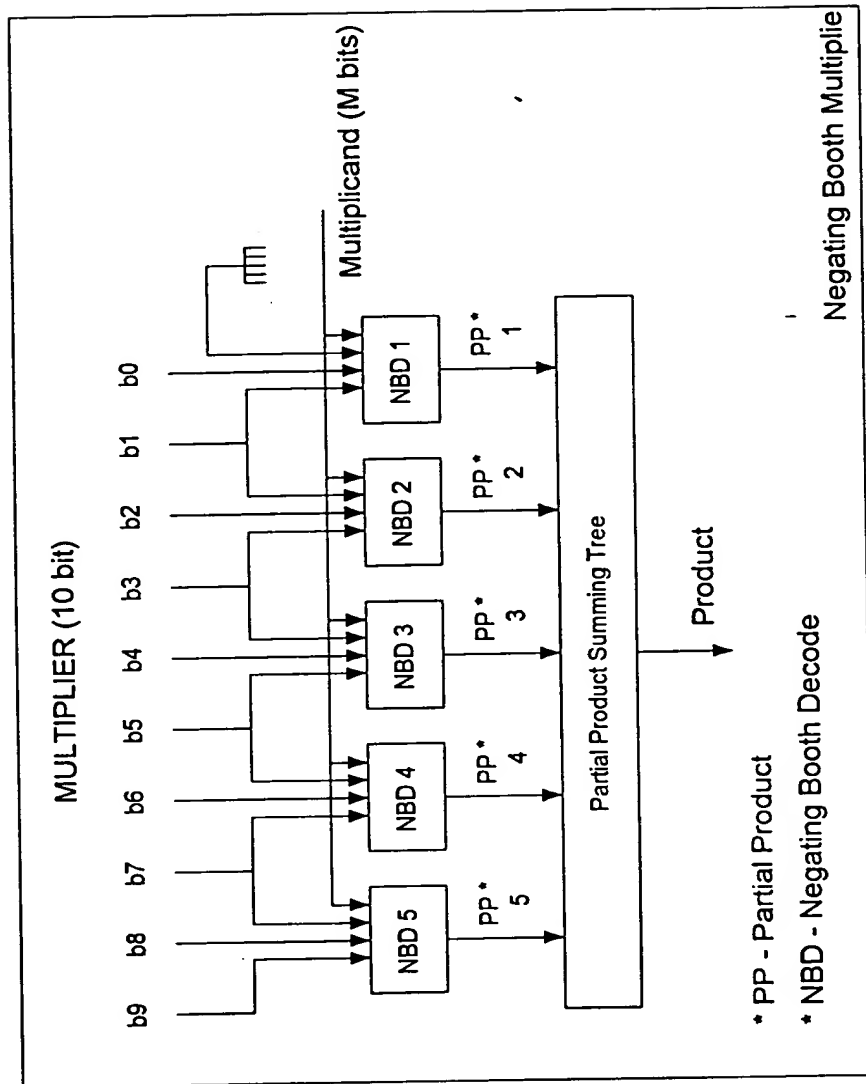


Fig. 52

5300

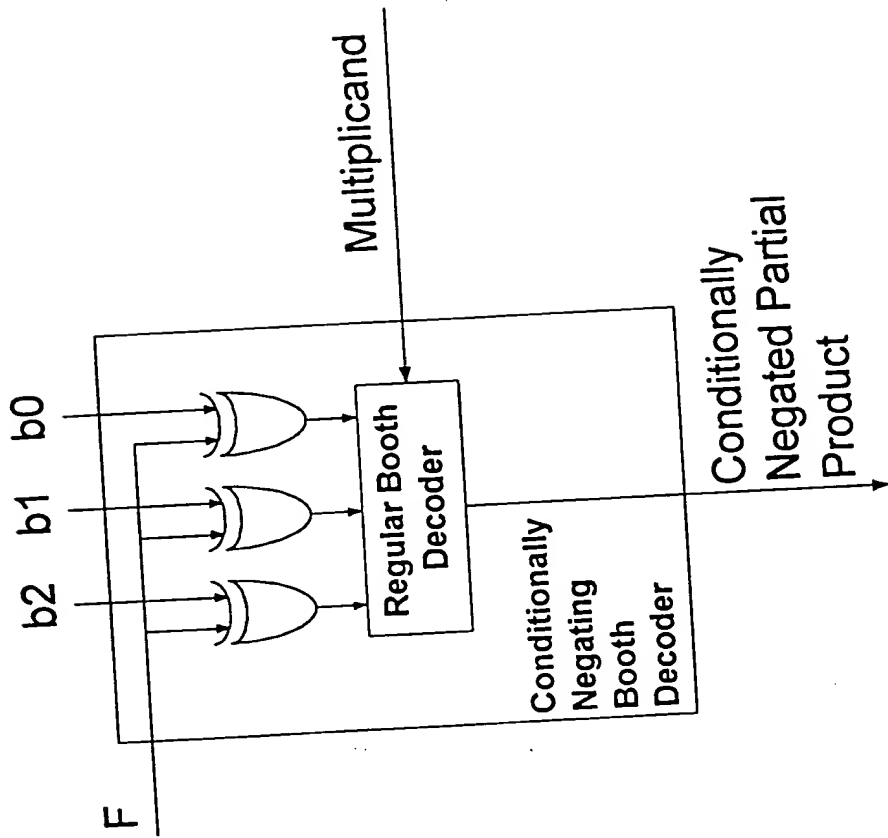


Fig. 53

5406

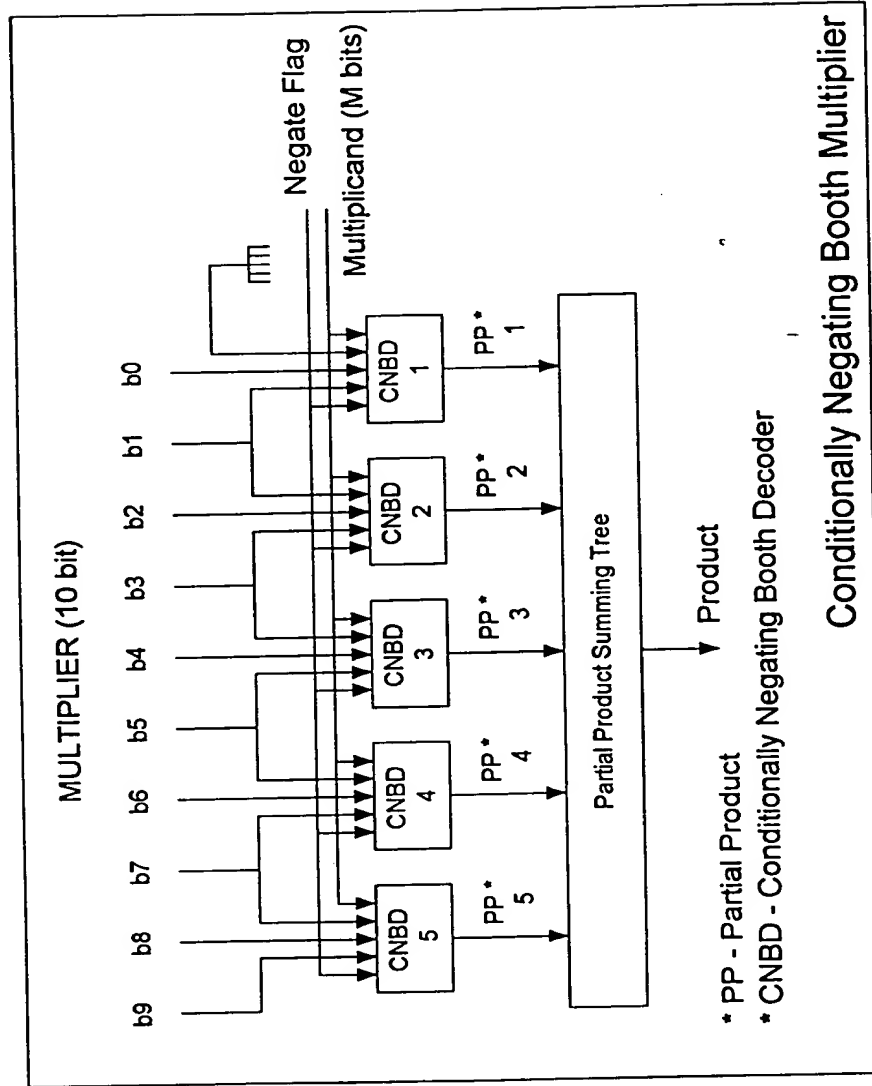


Fig. 54

5500

5502

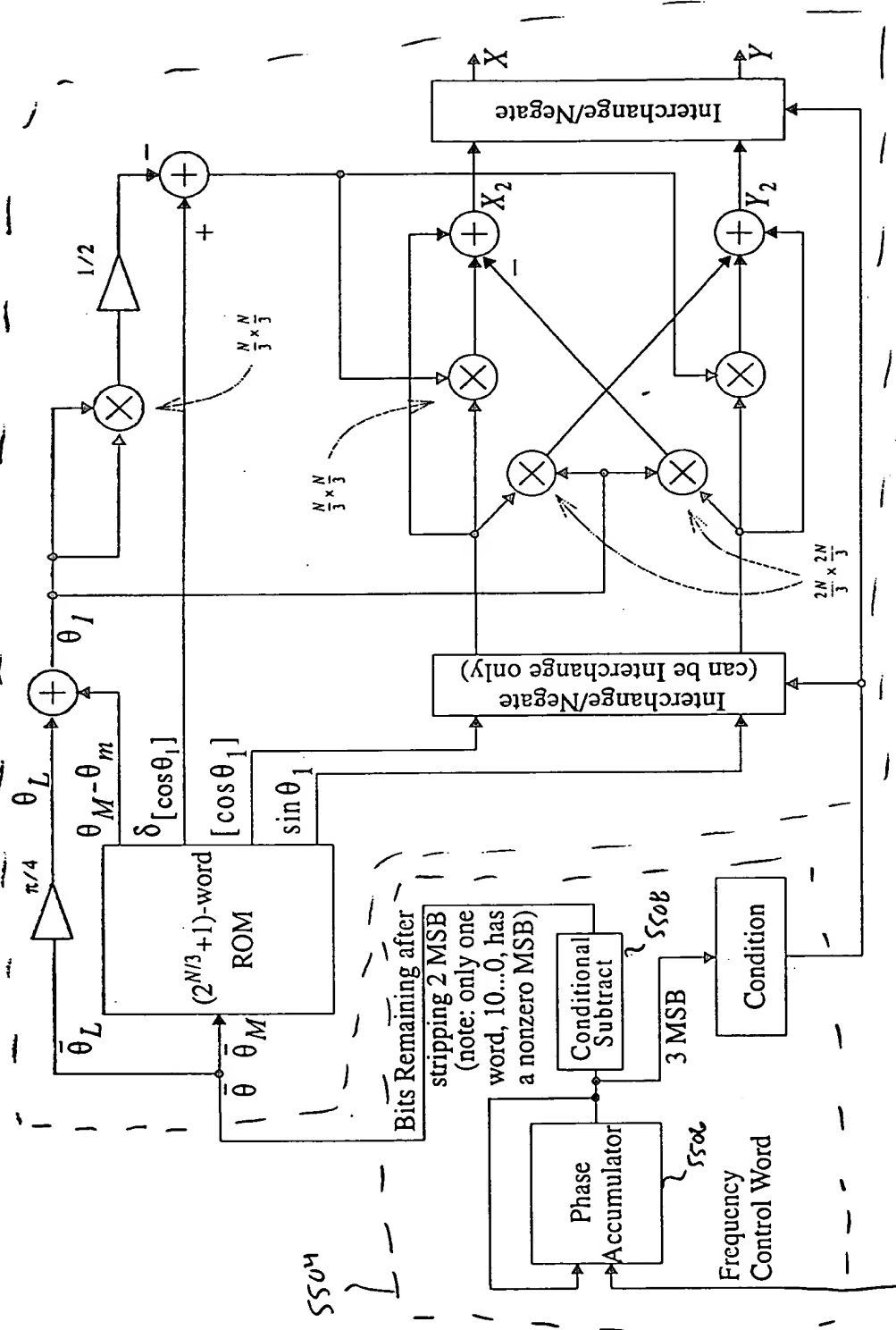


Fig. 55 Angle Rotator Configured as a Quadrature Direct Digital Synthesizer (QDDS).

5600

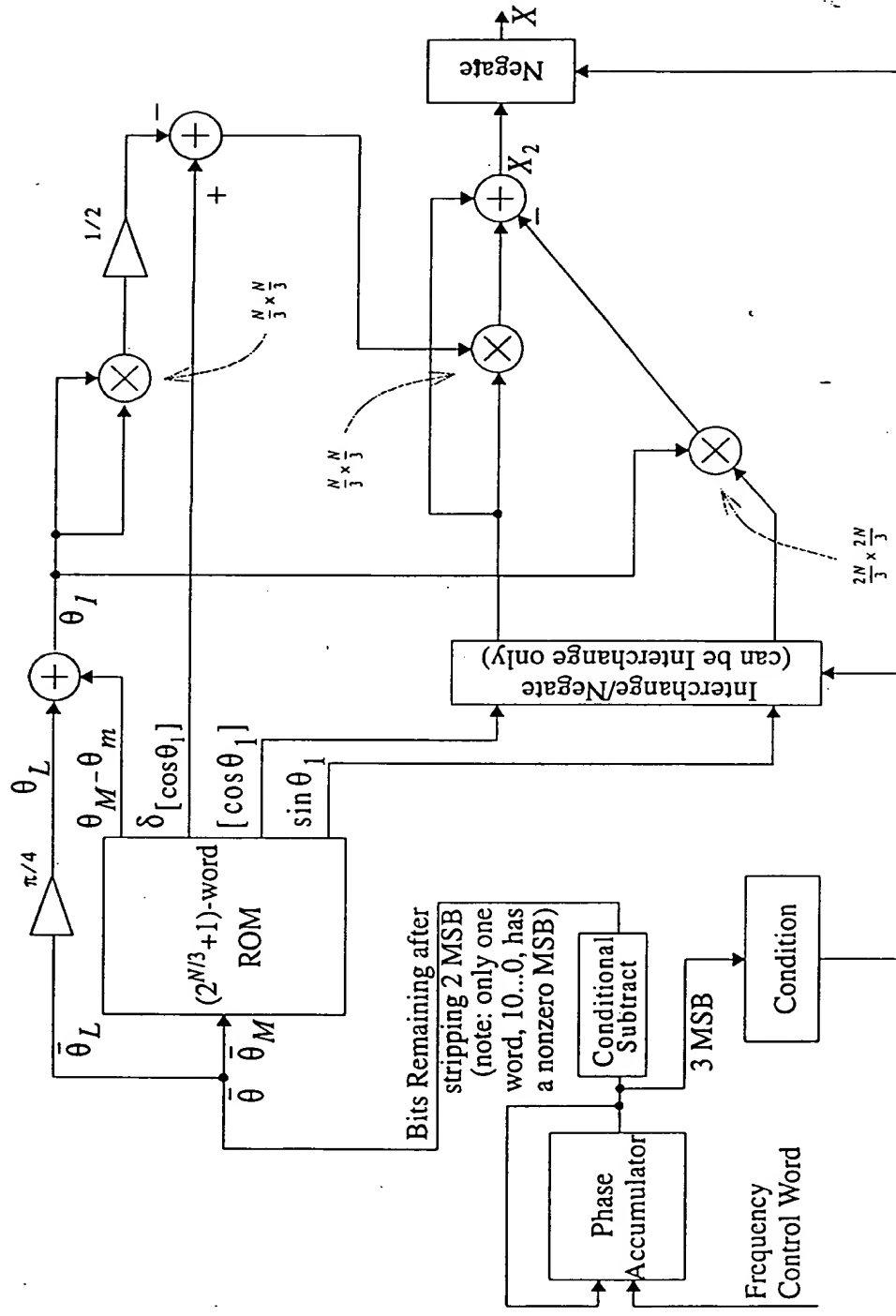


Fig. S6 Angle Rotator Configured as a "Cosine-only" Direct Digital Synthesizer (DDS) {from Fig 39}.



5802                      5804.

FIG. 58: Common packet format.

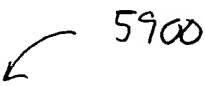


FIG. 59: The simplified system model.

000001-000000

FIG. 60 Mean values of the preamble correlator output, for  $\theta = 0$ .



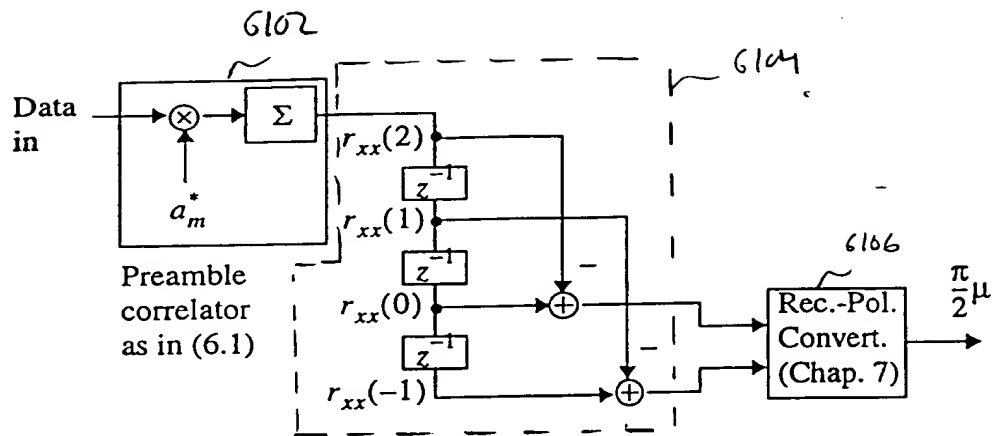


FIG. 610 Preliminary symbol-timing estimation structure.

6200  
↓

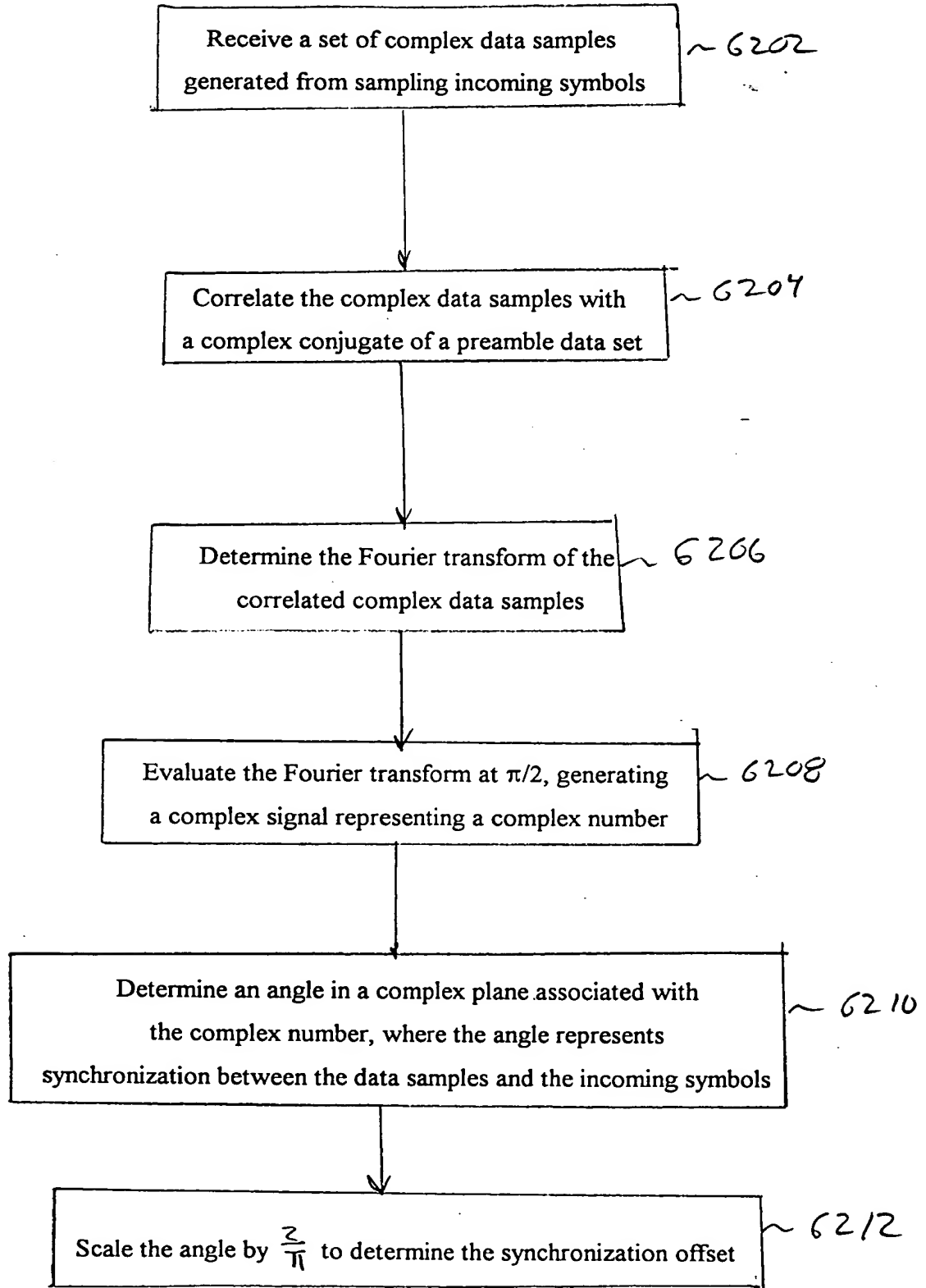


FIG. 62

000007 64286960

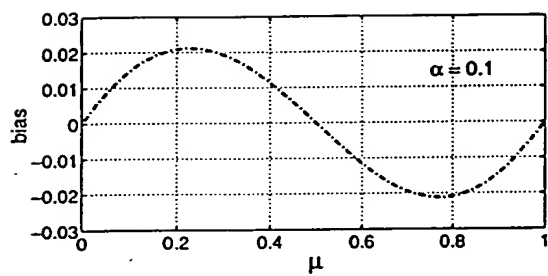


FIG. 63 Bias due to truncation.

6400

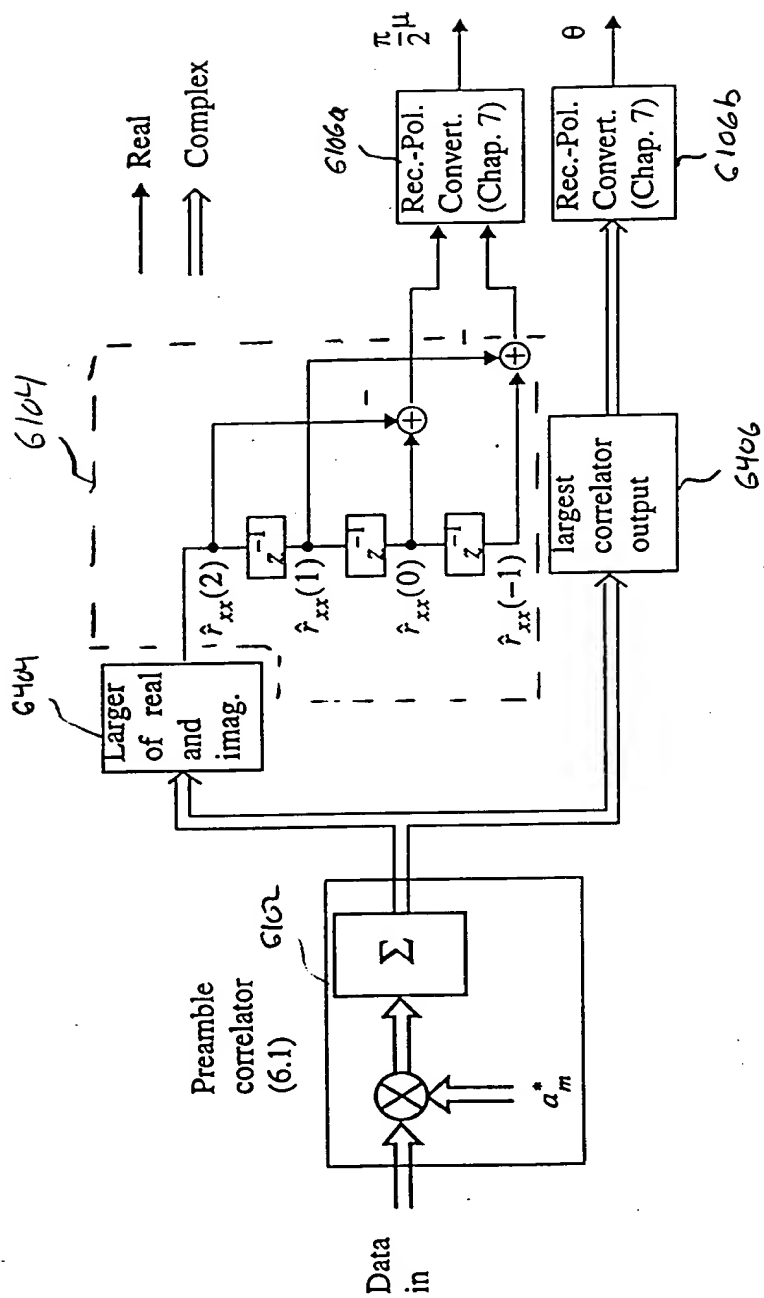


FIG. 64 Structure for carrier-phase and symbol timing recovery.

6500  
↓

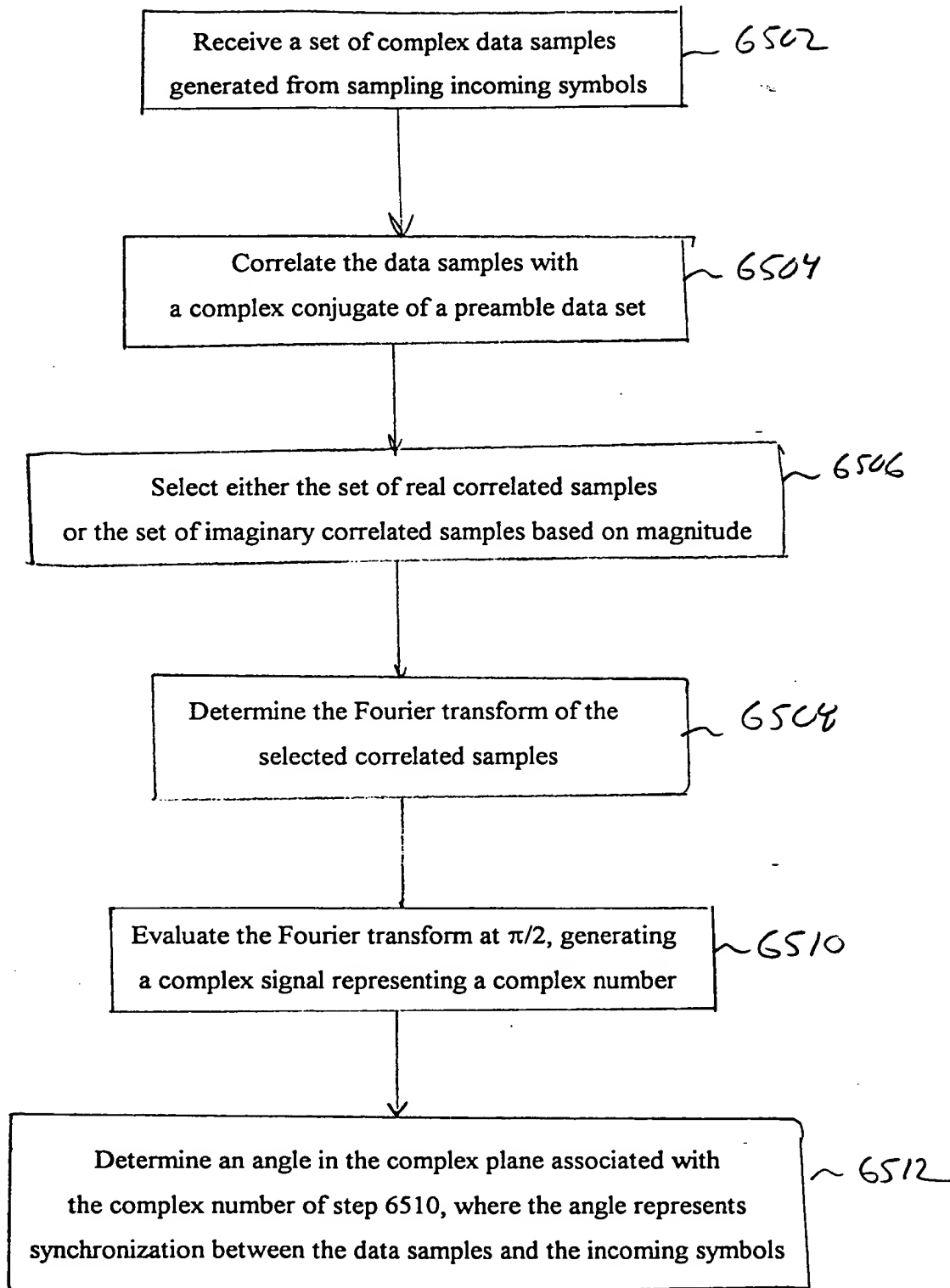


FIG. 65A

6500 (cont.)

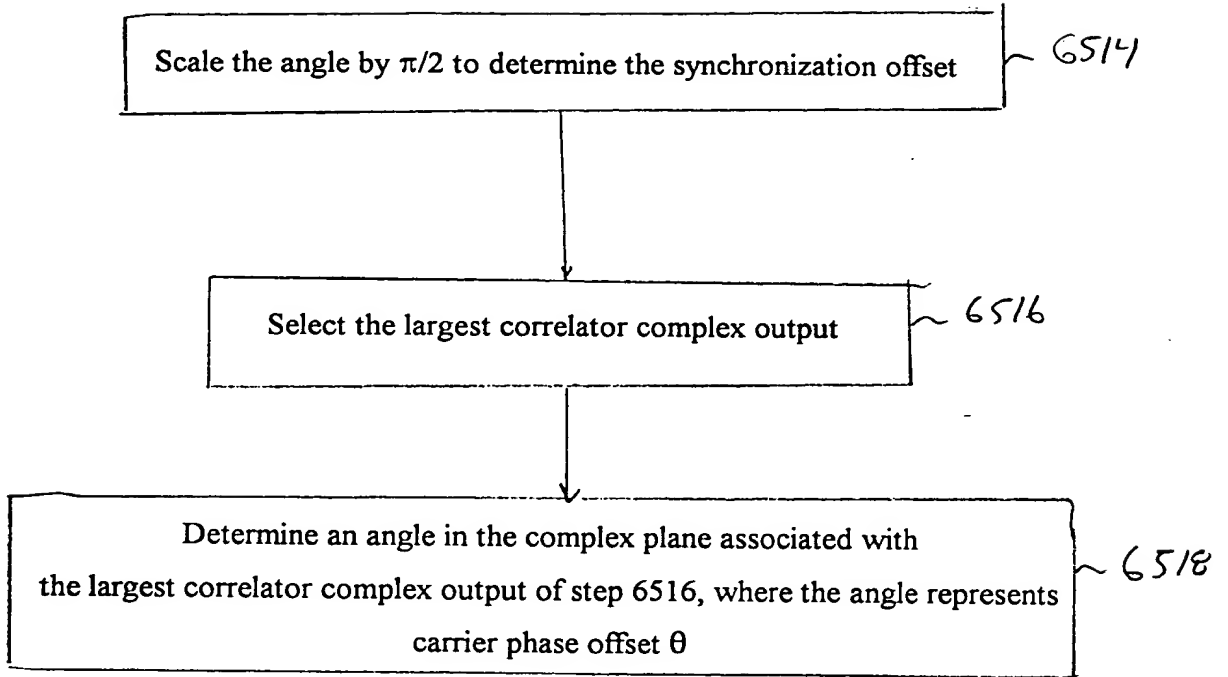


FIG. 65B

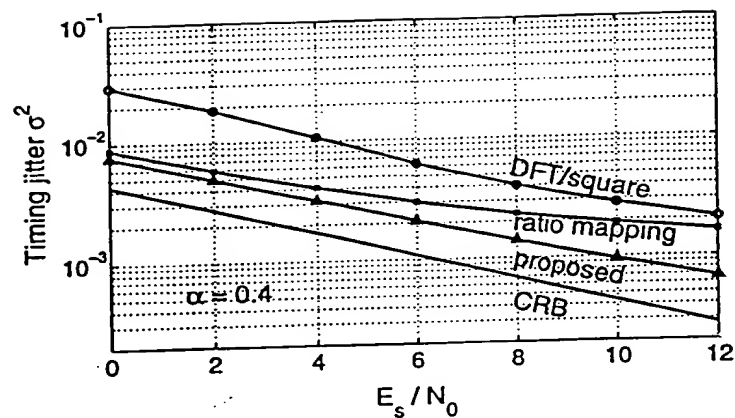


Figure 66: Timing jitter variance,  $\alpha = 0.4$ .

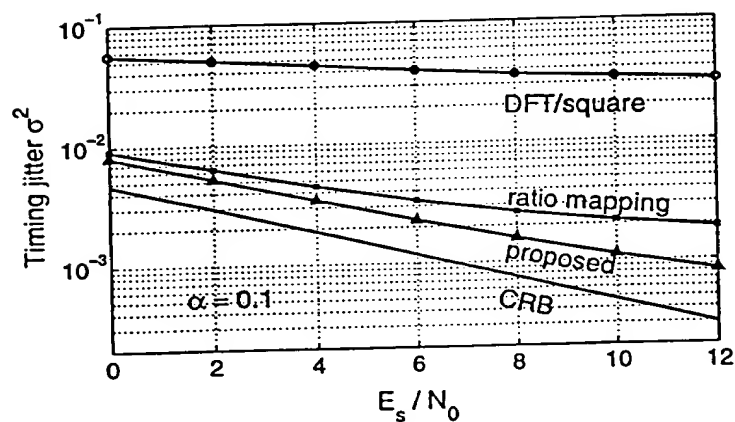


Figure 67: Timing jitter variance,  $\alpha = 0.1$ .

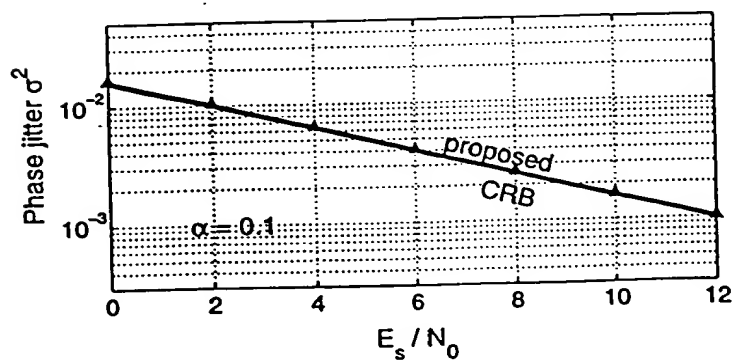


Figure 68: Phase jitter variance,  $\alpha = 0.1$ .

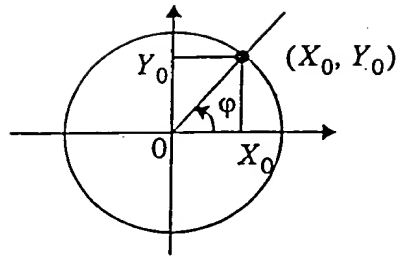


FIG. 67 Cartesian to polar conversion.



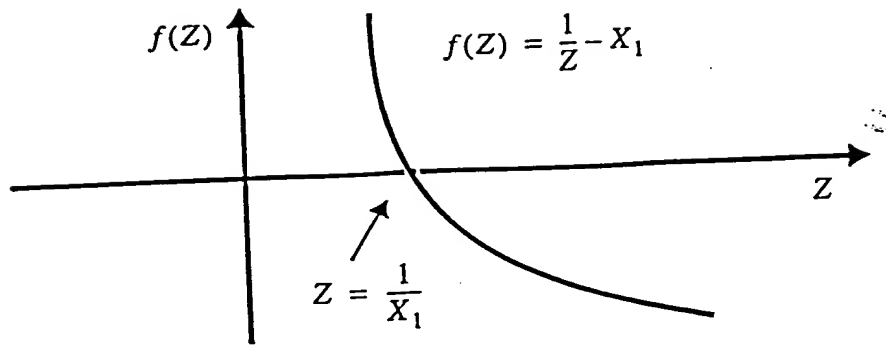


FIG. 70A: Using Newton-Raphson iteration to find  $1/X_1$ .

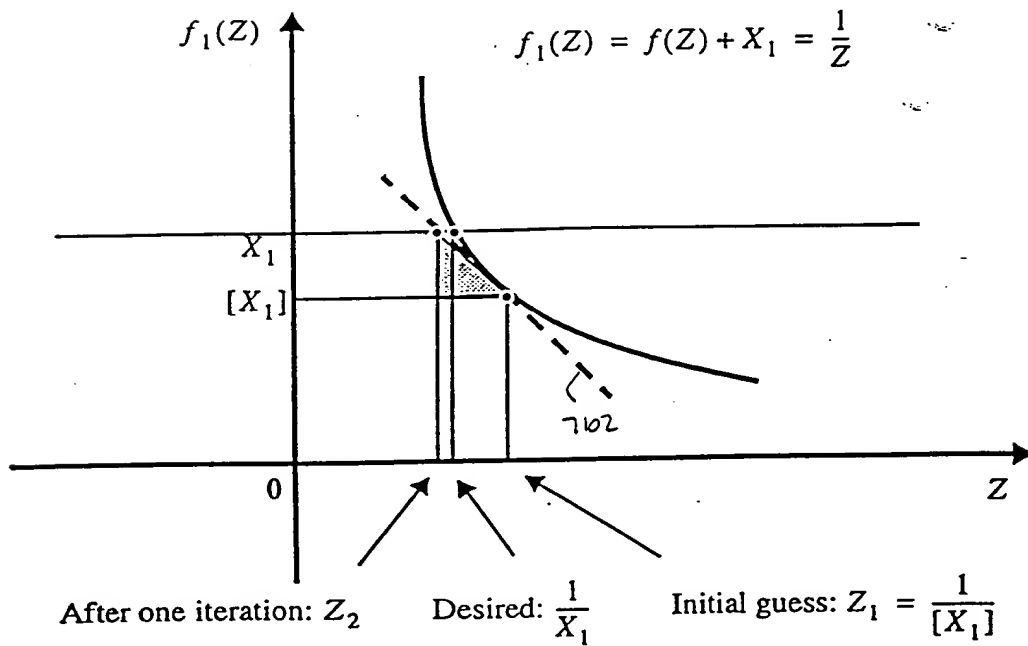


FIG. 70B: One Newton-Raphson iteration.

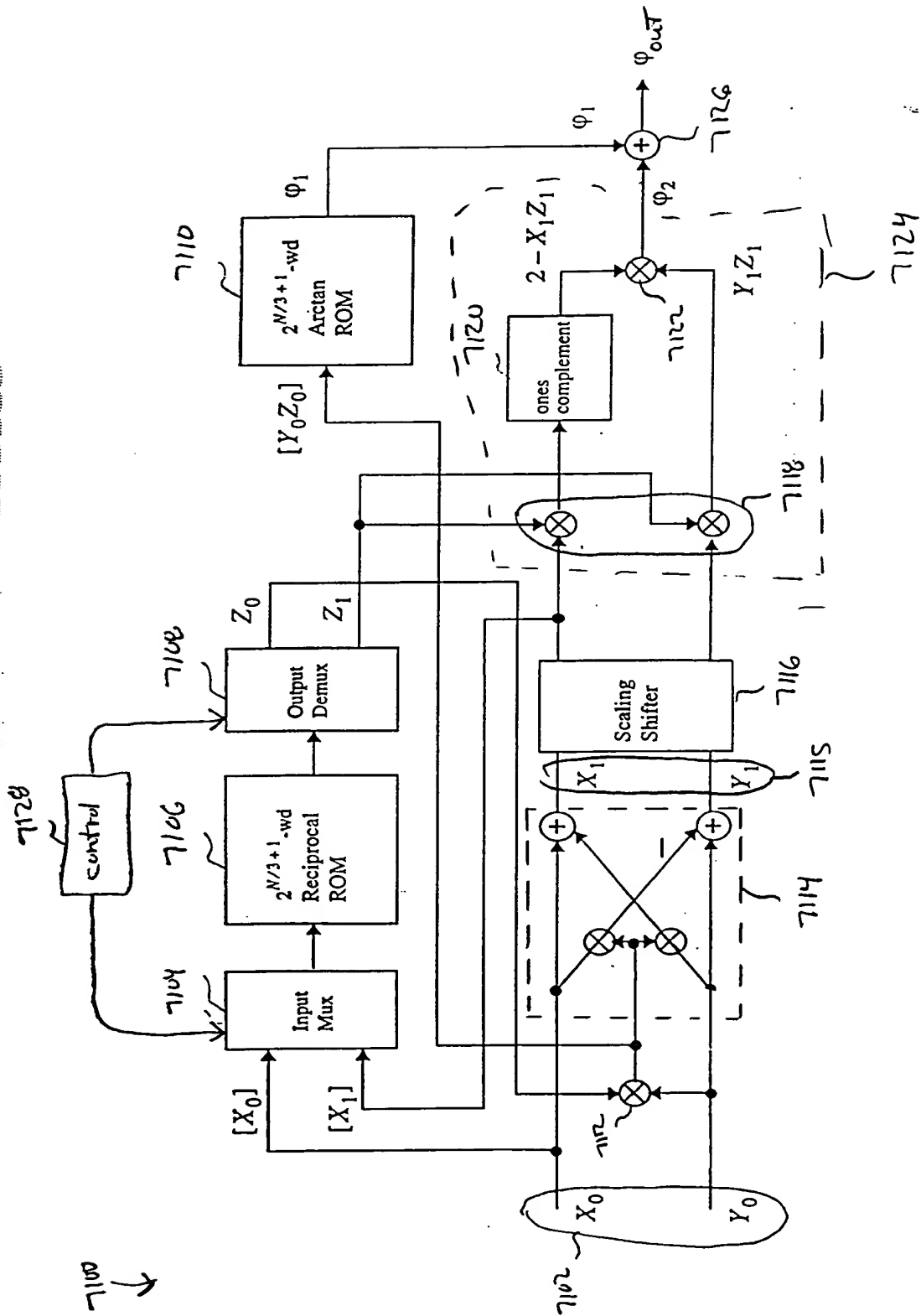


FIG. 71:

09698249 103000

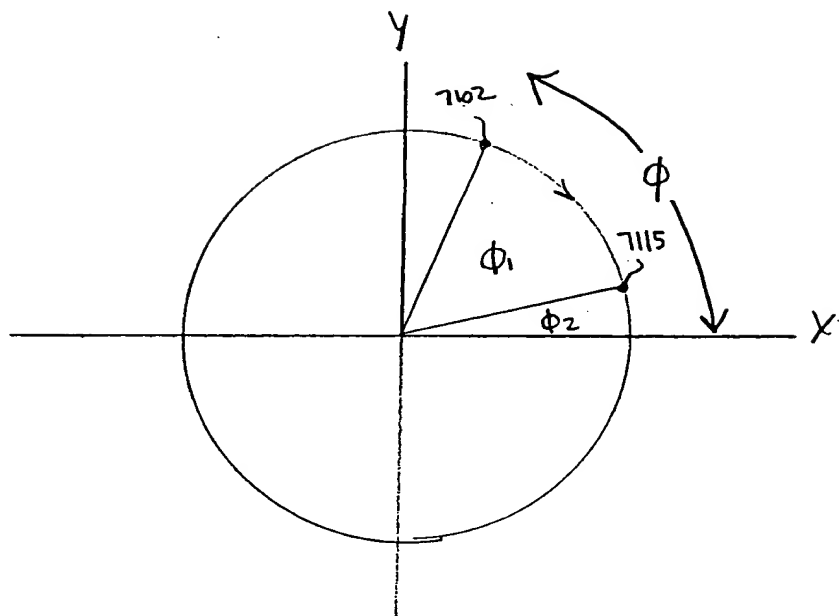
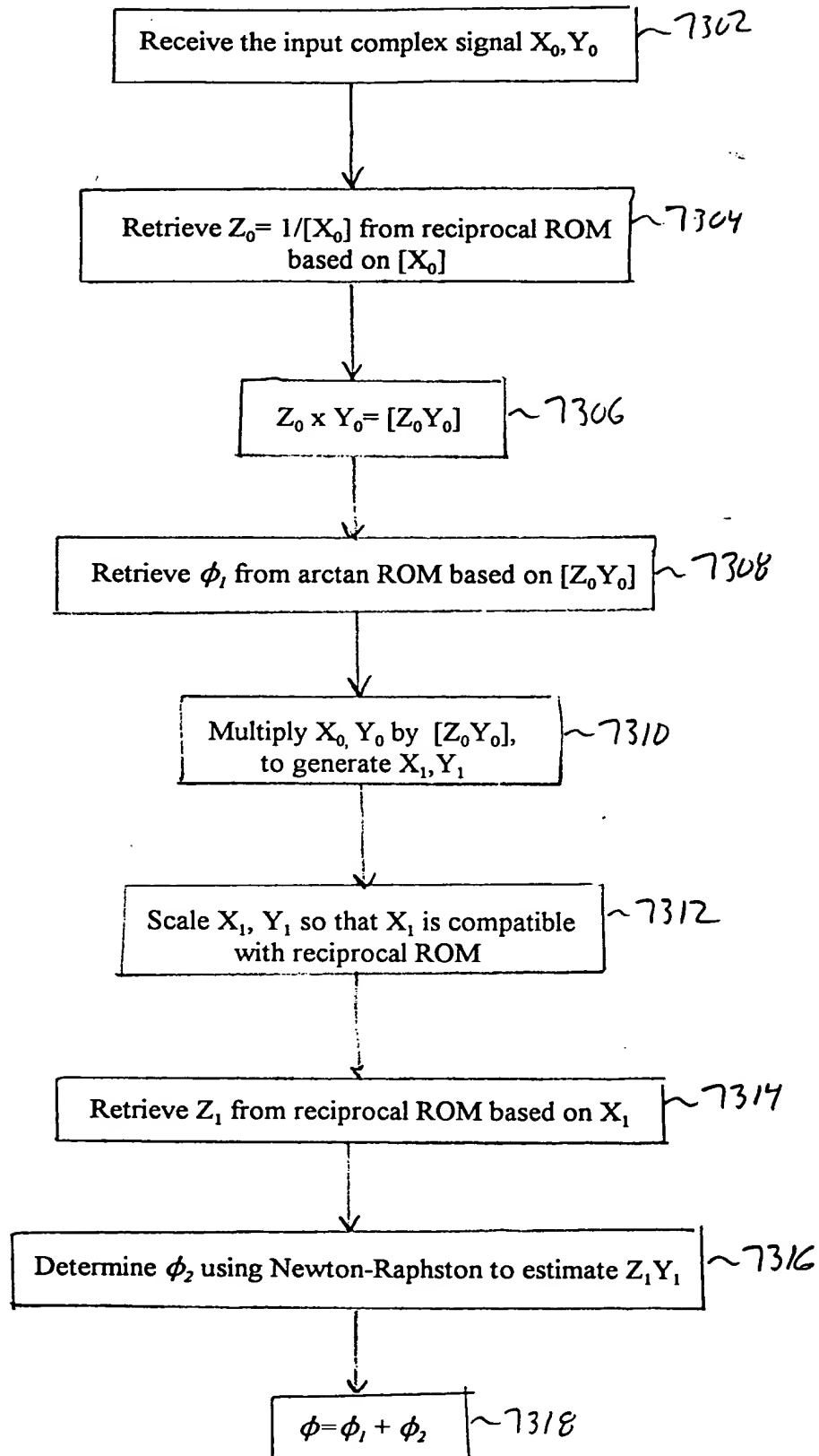


FIG. 72

00000000000000000000000000000000



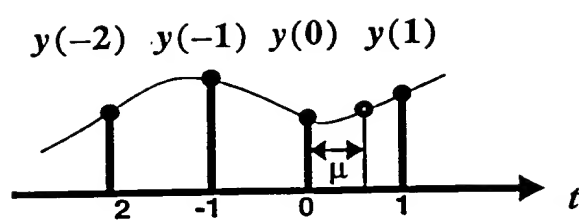


FIG. 74 Interpolation in a non-center interval.

FIG. 75A

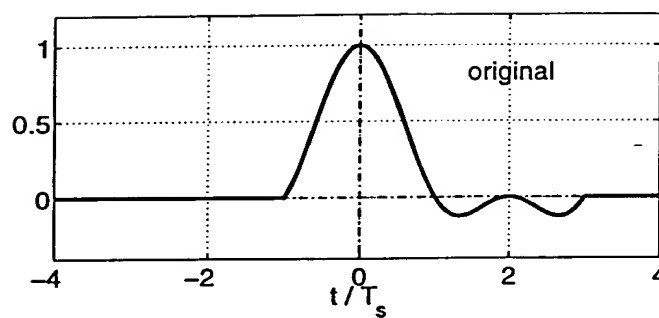


FIG 75B

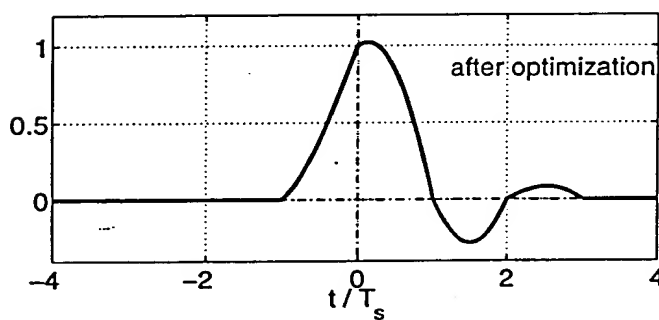


FIG. 75A-B: Impulse responses of the non-center-interval interpolation filter  $A$ , before and  $B$ , after optimization.

FIG. 76A

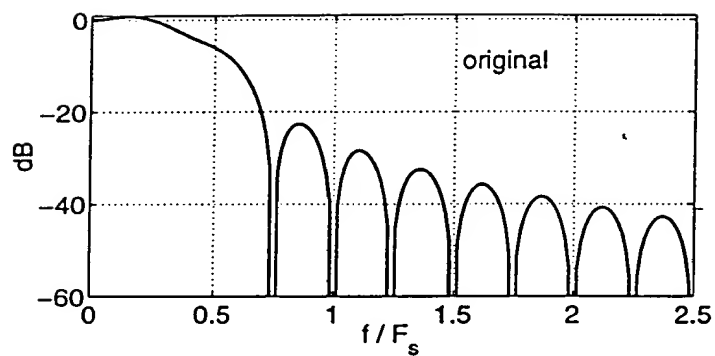


FIG. 76B

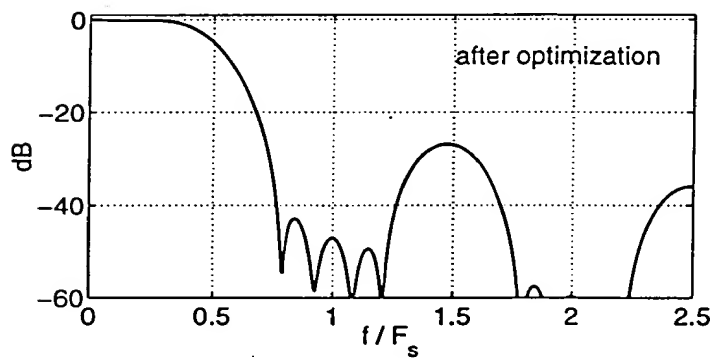


FIG. 76A-B : Frequency responses of the non-center-interval interpolator , before optimization and , after optimization.

The diagram illustrates a computer system 7702. A central vertical BUS 7706 is connected to several components:

- Peripherals (e.g. monitor, keyboard, mouse)** 7703: Connected to the top of the bus.
- PROCESSOR** 7704: Connected to the bus.
- MAIN MEMORY** 7708: Connected to the bus.
- A storage and interface block 7710, which contains:
  - HARD DRIVE** 7712: Connected to the bus.
  - REMOVABLE DRIVE** 7714: Connected to the bus and an external component 7716 via a dashed line.
  - INTERFACE** 7718: Connected to the bus and an external component 7720 via a dashed line.
- COMMUNICATION I/F** 7722: Connected to the bus and **External Devices** 7726 via a bidirectional arrow 7724.

Fig. 77



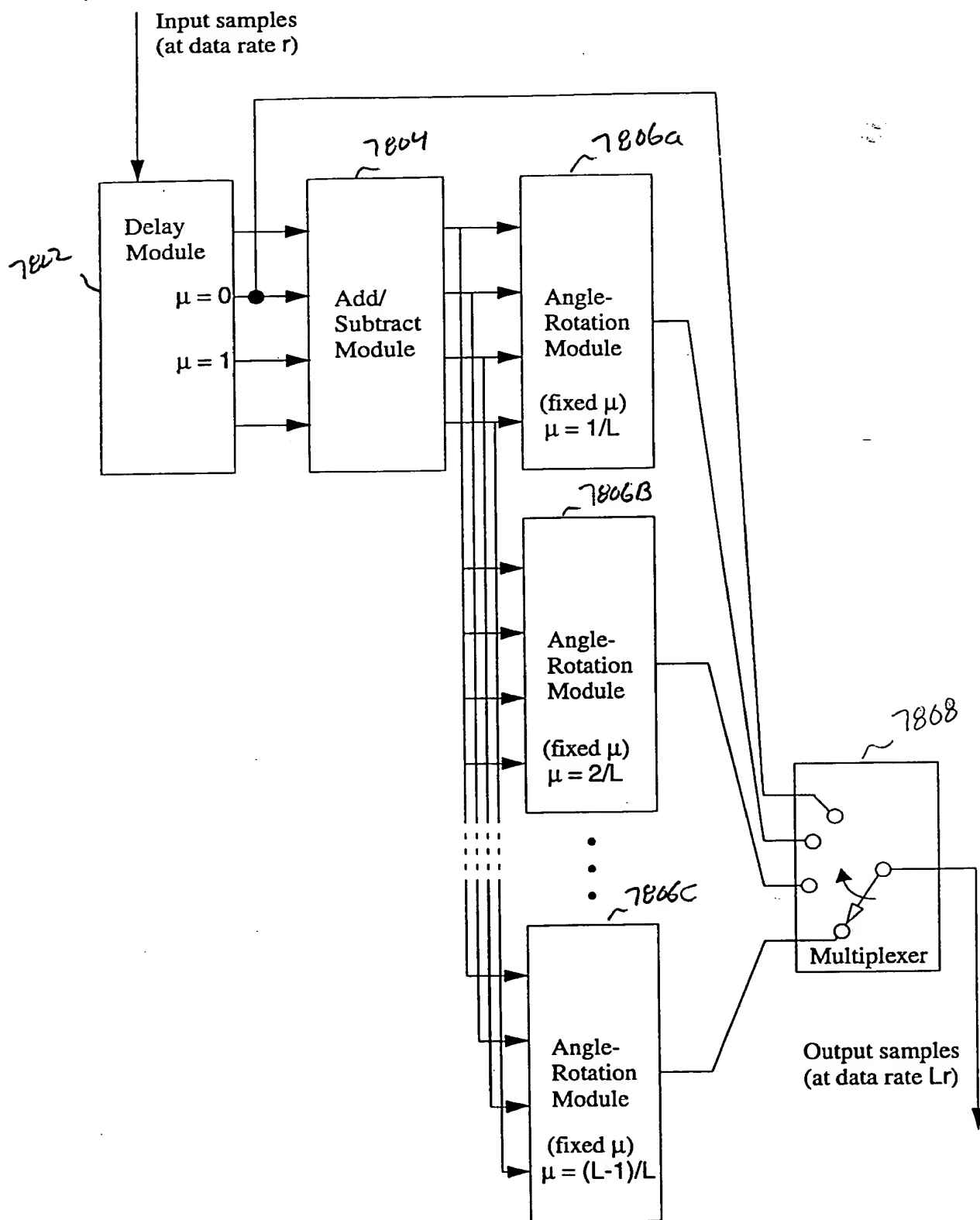


FIG. 78 Data Rate Expansion Circuit.